TL07xx Low-Noise FET-Input Operational Amplifiers

1 Features

- High slew rate: 20 V/µs (TL07xH, typ)
- Low offset voltage: 1 mV (TL07xH, typ)
- Low offset voltage drift: 2 µV/°C
- Low power consumption: 940 µA/ch (TL07xH, typ)
- Wide common-mode and differential voltage ranges
  - Common-mode input voltage range includes V_{CC+}
- Low input bias and offset currents
- Low noise:
  $V_n = 18\ nV/\sqrt{Hz}$ (typ) at f = 1 kHz
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)
- Wide supply voltage:
  ±2.25 V to ±20 V, 4.5 V to 40 V

2 Applications

- Solar energy: string and central inverter
- Motor drives: AC and servo drive control and power stage modules
- Single phase online UPS
- Three phase UPS
- Pro audio mixers
- Battery test equipment

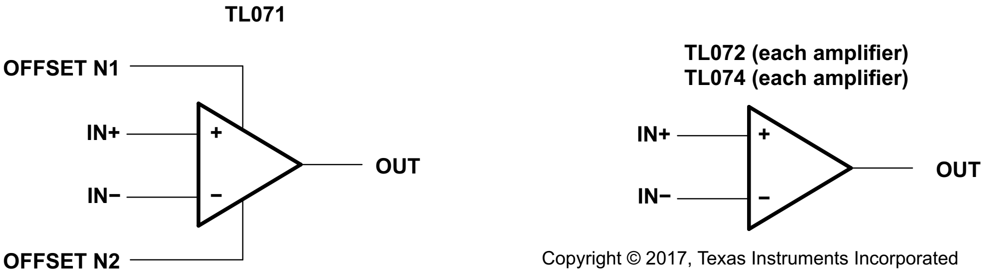
3 Description

The TL07xH (TL071H, TL072H, and TL074H) family of devices are the next-generation versions of the industry-standard TL07x (TL071, TL072, and TL074) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typical), high slew rate (20 V/µs), and common-mode input to the positive supply. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the TL07xH devices to be used in the most rugged and demanding applications.

Device Information

PART NUMBER[1]	PACKAGE	BODY SIZE (NOM)
TL071x	PDIP (8)	9.59 mm × 6.35 mm
	SC70 (5)	2.00 mm × 1.25 mm
	SO (8)	6.20 mm × 5.30 mm
	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (5)	1.60 mm × 1.20 mm
TL072x	PDIP (8)	9.59 mm × 6.35 mm
	SO (8)	6.20 mm × 5.30 mm
	SOIC (8)	4.90 mm × 3.90 mm
	SOT-23 (8)	2.90 mm × 1.60 mm
	TSSOP (8)	4.40 mm × 3.00 mm
TL072M	CDIP (8)	9.59 mm × 6.67 mm
	CFP (10)	6.12 mm × 3.56 mm
	LCCC (20)	8.89 mm × 8.89 mm
TL074x	PDIP (14)	19.30 mm × 6.35 mm
	SO (14)	10.30 mm × 5.30 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOT-23 (14)	4.20 mm × 2.00 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm
TL074M	CDIP (14)	19.56 mm × 6.92 mm
	CFP (14)	9.21 mm × 6.29 mm
	LCCC (20)	8.89 mm × 8.89 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Logic Symbols

Table of Contents

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision S (July 2021) to Revision T (December 2021) **Page**

- Corrected DCK pinout diagram and table in *Pin Configurations and Functions* section....5

Changes from Revision R (June 2021) to Revision S (July 2021) **Page**

- Deleted preview note from TL071H SOIC (8), SOT-23 (5) and SC70 (5) packages throughout the data sheet 1

Changes from Revision Q (June 2021) to Revision R (June 2021) **Page**

- Deleted preview note from TL072H SOIC (8), SOT-23 (8) and TSSOP (8) packages throughout the data sheet....1
- Added ESD information for TL072H....12
- Added I_Q spec for TL072H....17

Changes from Revision P (November 2020) to Revision Q (June 2021) **Page**

- Deleted VSSOP (8) package from the *Device Information* section....1

- Added DBV, DCK, and D packages to TL071H in *Pin Configuration and Functions* section............................5
- Deleted DGK package from TL072x in *Pin Configuration and Functions* section... 5
- Deleted tables with duplicate information from the *Specifications* section.. 12
- Added D, DCK, and DBV package thermal information in Thermal Information for Single Channel: TL071H section.. 13
- Added D, DDF, and PW package thermal information in Thermal Information for Dual Channel: TL072H section.. 14
- Added I_B and I_{OS} specification for single channel DCK and DBV package... 17
- Added I_Q spec for TL071H...17
- Deleted *Related Links* section from the *Device and Documentation Support* section...................................45

Changes from Revision O (October 2020) to Revision P (November 2020) — Page

- Added SOIC and TSSOP package thermal information in *Thermal Information for Quad Channel: TL074H section* 15
- Added *Typical Characteristics:TL07xH* section in *Specifications* section..26

Changes from Revision N (July 2017) to Revision O (October 2020) — Page

- Updated the numbering format for tables, figures, and cross-references throughout the document.................1
- Features of TL07xH added to the *Features* section... 1
- Added link to applications in the *Applications* section.. 1
- Added TL07xH in the *Description* section...1
- Added TL07xH device in the *Device Information* section.. 1
- Added SOT-23 (14), VSSOP (8), SOT-23 (8), SC70 (5), and SOT-23 (5) packages to the *Device Information* section.. 1
- Added TSSOP, VSSOP and DDF packages to TL072x in *Pin Configuration and Functions* section................. 5
- Added DYY package to TL074x in *Pin Configuration and Functions* section..5
- Removed Table of Graphs from the *Typical Characteistics* section...33
- Deleted reference to obsolete documentation in *Layout Guidelines* section...43
- Removed *Related Documentation* section.. 45

Changes from Revision M (February 2014) to Revision N (July 2017) — Page

- Updated data sheet text to latest documentation and translation standards... 1
- Added TL072M and TL074M devices to data sheet 1
- Rewrote text in *Description* section 1
- Changed TL07x 8-pin PDIP package to 8-pin CDIP package in *Device Information* table 1
- Deleted 20-pin LCCC package from *Device Information* table 1
- Added 2017 copyright statement to front page schematic...1
- Deleted TL071x FK (LCCC) pinout drawing and pinout table in *Pin Configurations and Functions* section 5
- Updated pinout diagrams and pinout tables in *Pin Configurations and Functions* section 5
- Deleted differential input voltage parameter from *Absolute Maximum Ratings* table 12
- Deleted table notes from *Absolute Maximum Ratings* table 12
- Added new table note to *Absolute Maximum Ratings* table 12
- Changed minimum supply voltage value from –18 V to –0.3 V in *Absolute Maximum Ratings* table...............12
- Changed maximum supply voltage from 18 V to 36 V in *Absolute Maximum Ratings* table........................... 12
- Changed minimum input voltage value from –15 V to V_{CC-} – 0.3 V in *Absolute Maximum Ratings* table....... 12
- Changed maximum input voltage from 15 V to V_{CC-} + 36 V in *Absolute Maximum Ratings* table...................12
- Added input clamp current parameter to *Absolute Maximum Ratings* table 12
- Changed common-mode voltage maximum value from V_{CC+} – 4 V to V_{CC+} in the *Recommended Operating Conditions* table...13
- Changed devices in *Recommended Operating Conditions* table from TL07xA and TL07xB to TL07xAC and TL07xBC 13

- Added TL07xI operating free-air temperature minimum value of –40°C to *Recommended Operating Conditions* table 13
- Added U (CFP) package thermal values to *Thermal Information: TL072x (cont.)* table........ 15
- Added W (CFP) package thermal values to *Thermal Information: TL074x (cont.)* table........ 16
- Added Figure 6-59 to *Typical Characteristics* section........ 33
- Added second *Typical Application* section application curves 41
- Reformatted document references in *Layout Guidelines* section 43

Changes from Revision L (February 2014) to Revision M (February 2014) **Page**

- Added *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section........ 1

Changes from Revision K (January 2014) to Revision L (February 2014) **Page**

- Moved T_{stg} to *Handling Ratings* table 13

5 Pin Configuration and Functions

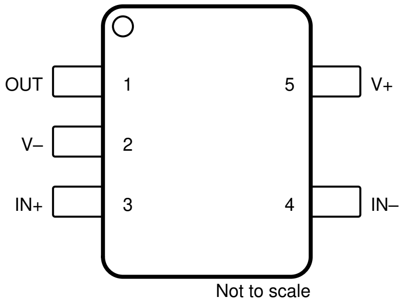


Figure 5-1. TL071H DBV Package
5-Pin SOT-23
(Top View)

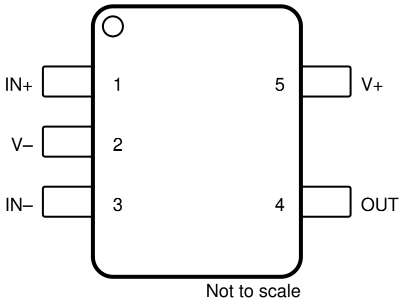
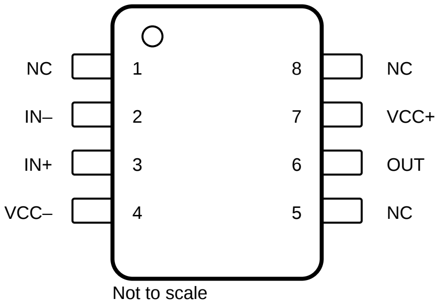


Figure 5-2. TL071H DCK Package
5-Pin SC70
(Top View)

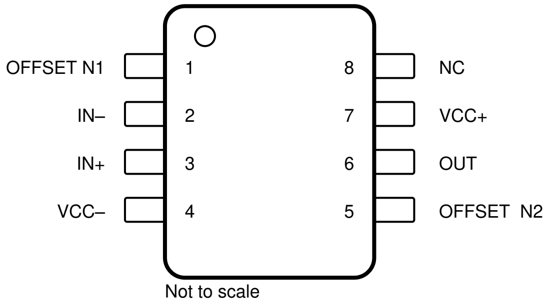


NC- no internal connection

Figure 5-3. TL071H D Package
8-Pin SOIC
(Top View)

Table 5-1. Pin Functions: TL071H

PIN				I/O	DESCRIPTION
NAME	DBV	DCK	D		
IN–	4	3	2	I	Inverting input
IN+	3	1	3	I	Noninverting input
NC	—	—	8	—	Do not connect
NC	—	—	1	—	Do not connect
NC	—	—	5	—	Do not connect
OUT	1	4	6	O	Output
VCC–	2	2	4	—	Power supply
VCC+	5	5	7	—	Power supply



NC- no internal connection

Figure 5-4. TL071x D, P, and PS Package 8-Pin SOIC, PDIP, and SO (Top View)

Table 5-2. Pin Functions: TL071x

PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	2	I	Inverting input
IN+	3	I	Noninverting input
NC	8	—	Do not connect
OFFSET N1	1	—	Input offset adjustment
OFFSET N2	5	—	Input offset adjustment
OUT	6	O	Output
VCC–	4	—	Power supply
VCC+	7	—	Power supply

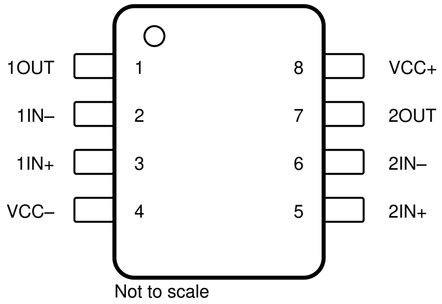
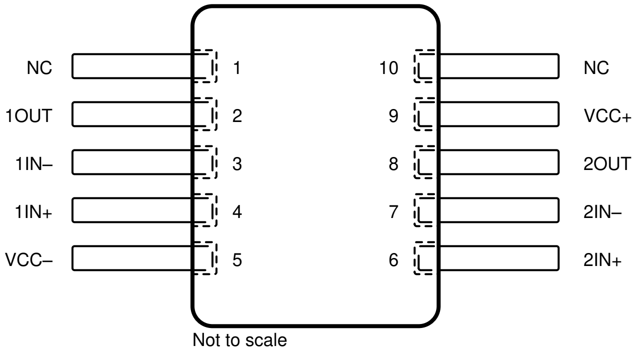


Figure 5-5. TL072x D, DDF, JG, P, PS, and PW Package 8-Pin SOIC, SOT-23 (8), CDIP, PDIP, SO, and TSSOP (Top View)

Table 5-3. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
VCC–	4	—	Power supply
VCC+	8	—	Power supply

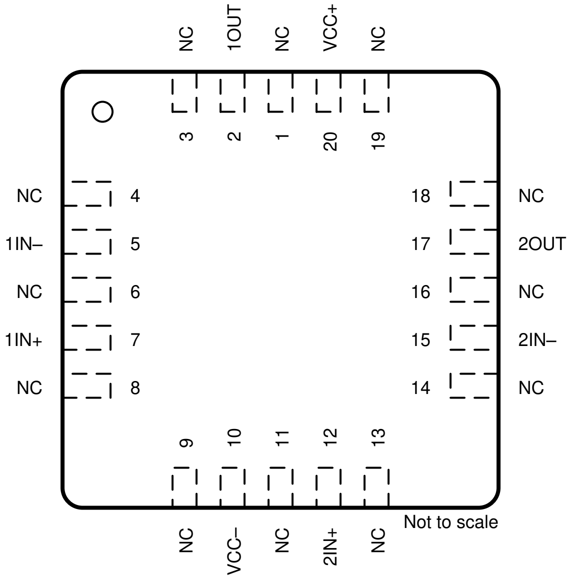


NC- no internal connection

Figure 5-6. TL072x U Package
10-Pin CFP
(Top View)

Table 5-4. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN–	7	I	Inverting input
2IN+	6	I	Noninverting input
2OUT	8	O	Output
NC	1, 10	—	Do not connect
VCC–	5	—	Power supply
VCC+	9	—	Power supply



NC- no internal connection

Figure 5-7. TL072 FK Package
20-Pin LCCC
(Top View)

Table 5-5. Pin Functions: TL072x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	5	I	Inverting input
1IN+	7	I	Noninverting input
1OUT	2	O	Output
2IN–	15	I	Inverting input
2IN+	12	I	Noninverting input
2OUT	17	O	Output
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	—	Do not connect
VCC–	10	—	Power supply
VCC+	20	—	Power supply

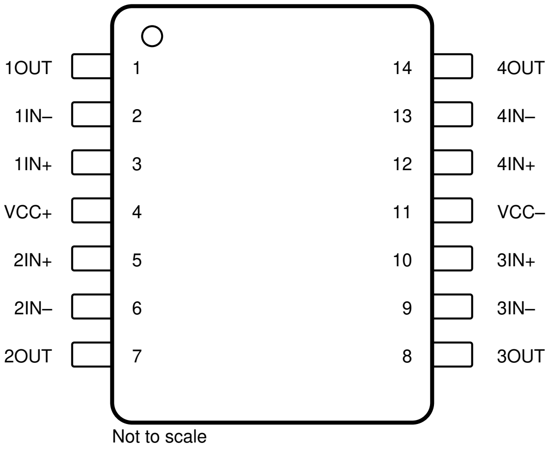
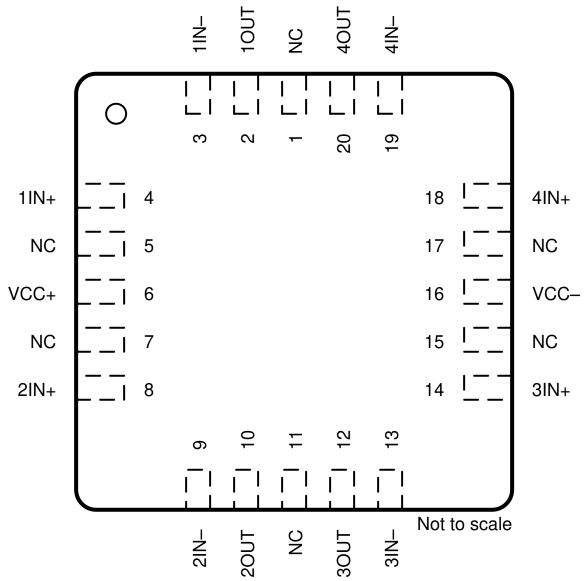


Figure 5-8. TL074x D, N, NS, PW, J, DYY, and W Package 14-Pin SOIC, PDIP, SO, TSSOP, CDIP, SOT-23 (14), and CFP (Top View)

Table 5-6. Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	2	I	Inverting input
1IN+	3	I	Noninverting input
1OUT	1	O	Output
2IN–	6	I	Inverting input
2IN+	5	I	Noninverting input
2OUT	7	O	Output
3IN–	9	I	Inverting input
3IN+	10	I	Noninverting input
3OUT	8	O	Output
4IN–	13	I	Inverting input
4IN+	12	I	Noninverting input
4OUT	14	O	Output
V_{CC-}	11	—	Power supply
V_{CC+}	4	—	Power supply



NC- no internal connection

**Figure 5-9. TL074 FK Package
20-Pin LCCC
(Top View)**

Table 5-7. Pin Functions: TL074x

PIN		I/O	DESCRIPTION
NAME	NO.		
1IN–	3	I	Inverting input
1IN+	4	I	Noninverting input
1OUT	2	O	Output
2IN–	9	I	Inverting input
2IN+	8	I	Noninverting input
2OUT	10	O	Output
3IN–	13	I	Inverting input
3IN+	14	I	Noninverting input
3OUT	12	O	Output
4IN–	19	I	Inverting input
4IN+	18	I	Noninverting input
4OUT	20	O	Output
NC	1, 5, 7, 11, 15, 17	—	Do not connect
VCC–	16	—	Power supply
VCC+	6	—	Power supply

6 Specifications

6.1 Absolute Maximum Ratings: TL07xH

over operating ambient temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, $V_S = (V_{CC+}) - (V_{CC-})$		0	42	V
Signal input pins	Common-mode voltage (3)	$(V_{CC-}) - 0.5$	$(V_{CC+}) + 0.5$	V
	Differential voltage (3)		$V_S + 0.2$	V
	Current (3)	–10	10	mA
Output short-circuit (2)		Continuous		
Operating ambient temperature, T_A		–55	150	°C
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.
(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

6.2 Absolute Maximum Ratings: All Devices Except TL07xH

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC+} - V_{CC-}	Supply voltage	–0.3	36	V
V_I	Input voltage (3)	$V_{CC-} - 0.3$	$V_{CC-} + 36$	V
I_{IK}	Input clamp current		–50	mA
	Duration of output short circuit(2)	Unlimited		
T_J	Operating virtual junction temperature		150	°C
	Case temperature for 60 seconds - FK package		260	°C
	Lead temperature 1.8 mm (1/16 inch) from case for 10 seconds		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The output may be shorted to ground or to either supply. Temperature and supply voltages must be limited to ensure that the dissipation rating is not exceeded.
(3) Differential voltage only limited by input voltage.

6.3 ESD Ratings: TL07xH

			VALUE	UNIT
TL074H				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
TL072H and TL071H				
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 ESD Ratings: All Devices Except TL07xH

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.5 Recommended Operating Conditions: TL07xH

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage, $(V_{CC+}) – (V_{CC–})$	4.5	40	V
V_I	Input voltage range	$(V_{CC–}) + 2$	$(V_{CC+}) + 0.1$	V
T_A	Specified temperature	–40	125	°C

6.6 Recommended Operating Conditions: All Devices Except TL07xH

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC+}	Supply voltage (1)		5	15	V
$V_{CC–}$	Supply voltage (1)		–5	–15	V
V_{CM}	Common-mode voltage		$V_{CC–} + 4$	V_{CC+}	V
T_A	Operating free-air temperature	TL07xM	–55	125	°C
		TL08xQ	–40	125	
		TL07xI	–40	85	
		TL07xAC, TL07xBC, TL07xC	0	70	

(1) V_{CC+} and $V_{CC–}$ are not required to be of equal magnitude, provided that the total V_{CC} $(V_{CC+} – V_{CC–})$ is between 10 V and 30 V.

6.7 Thermal Information for Single Channel: TL071H

THERMAL METRIC (1)		TL071H			UNIT
		D (SOIC)	DCK (SC70)	DBV (SOT-23)	
		8 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	158.8	217.5	212.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	98.6	113.1	111.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	102.3	63.8	79.4	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	45.8	34.8	51.8	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	101.5	63.5	79.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.8 Thermal Information: TL071x

THERMAL METRIC[1]		TL071x			UNIT
		D (SOIC)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.9 Thermal Information for Dual Channel: TL072H

THERMAL METRIC (1)		TL072H			UNIT
		D (SOIC)	DDF (SOT-23)	PW (TSSOP)	
		8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	147.8	181.5	200.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	88.2	112.5	89.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.4	98.2	131.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	36.8	17.2	22.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	90.6	97.6	129.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.10 Thermal Information: TL072x

THERMAL METRIC[1]		TL072x				UNIT
		D (SOIC)	JG (CDIP)	P (PDIP)	PS (SO)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	—	85	95	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	15.05	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.11 Thermal Information: TL072x (cont.)

THERMAL METRIC[1]		TL072x			UNIT
		PW (TSSOP)	U (CFP)	FK (LCCC)	
		8 PINS	10 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150	169.8	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	62.1	5.61	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	176.2	—	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	—	48.4	—	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	—	144.1	—	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	5.4	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.12 Thermal Information for Quad Channel: TL074H

THERMAL METRIC [1]		TL074H			UNIT
		D (SOIC)	DYY [2] (SOT-23)	PW (TSSOP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.2	TBD	134.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	70.3	TBD	62.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	70.2	TBD	77.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	28.8	TBD	13.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	69.8	TBD	77.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	TBD	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

(2) This package option is preview for TL074H.

6.13 Thermal Information: TL074x

THERMAL METRIC[1]		TL074x			UNIT
		D (SOIC)	N (PDIP)	NS (SO)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	86	80	76	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.14 Thermal Information: TL074x (cont).

THERMAL METRIC(1)		TL074x			UNIT
		J (CDIP)	PW (TSSOP)	W (CFP)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	113	128.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	14.5	—	56.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	—	—	127.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	—	—	29	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	—	—	106.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.15 Thermal Information: TL074x (cont).

THERMAL METRIC(1)		TL074x	UNIT
		FK (LCCC)	
		20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	—	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	5.61	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.16 Thermal Information

THERMAL METRIC(1)		TL071/TL072/TL074											UNIT
		D (SOIC)		FK (LCCC)	J (CDIP)		N (PDIP)		NS (SO)		PW (TSSOP)		
		8 PINS	14 PINS	20 PINS	8 PINS	14 PINS	8 PINS	14 PINS	8 PINS	14 PINS	8 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	97	86	—	—	—	85	80	95	76	150	113	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	—	—	5.61	15.05	14.5	—	—	—	—	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.17 Electrical Characteristics: TL07xH

For $V_S = (V_{CC+}) – (V_{CC–})$ = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, $V_{CM} = V_S$ / 2, and $V_{OUT} = V_S$ / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V_{OS}	Input offset voltage				±1	±4	mV
			T_A = –40°C to 125°C			±5	
dV_{OS}/dT	Input offset voltage drift		T_A = –40°C to 125°C		±2		μV/℃
PSRR	Input offset voltage versus power supply	V_S = 5 V to 40 V, $V_{CM} = V_S$ / 2	T_A = –40°C to 125°C		±1	±10	μV/V
	Channel separation	f = 0 Hz			10		μV/V
INPUT BIAS CURRENT							
I_B	Input bias current				±1	±120	pA
			DCK and DBV packages		±1	±300	pA
			T_A = –40°C to 125°C [1]			±5	nA
I_{OS}	Input offset current				±0.5	±120	pA
			DCK and DBV packages		±0.5	±250	pA
			T_A = –40°C to 125°C [1]			±5	nA
NOISE							
E_N	Input voltage noise	f = 0.1 Hz to 10 Hz			9.2		μV_{PP}
					1.4		μV_{RMS}
e_N	Input voltage noise density	f = 1 kHz			37		nV/√Hz
		f = 10 kHz			21		
i_N	Input current noise	f = 1 kHz			80		fA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-mode voltage range			$(V_{CC–})$ + 1.5		(V_{CC+})	V
CMRR	Common-mode rejection ratio	V_S = 40 V, $(V_{CC–})$ + 2.5 V < V_{CM} < (V_{CC+}) – 1.5 V		100	105		dB
CMRR	Common-mode rejection ratio		T_A = –40°C to 125°C	95			dB
CMRR	Common-mode rejection ratio	V_S = 40 V, $(V_{CC–})$ + 2.5 V < V_{CM} < (V_{CC+})		90	105		dB
CMRR	Common-mode rejection ratio		T_A = –40°C to 125°C	80			dB
INPUT CAPACITANCE							
Z_{ID}	Differential				100 || 2		MΩ || pF
Z_{ICM}	Common-mode				6 || 1		TΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S$ / 2, $(V_{CC–})$ + 0.3 V < V_O < (V_{CC+}) – 0.3 V	T_A = –40°C to 125°C	118	125		dB
A_{OL}	Open-loop voltage gain	V_S = 40 V, $V_{CM} = V_S$ / 2, R_L = 2 kΩ, $(V_{CC–})$ + 1.2 V < V_O < (V_{CC+}) – 1.2 V	T_A = –40°C to 125°C	115	120		dB
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product				5.25		MHz
SR	Slew rate	V_S = 40 V, G = +1, C_L = 20 pF			20		V/μs
t_S	Settling time	To 0.1%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			0.63		μs
		To 0.1%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			0.56		
		To 0.01%, V_S = 40 V, V_{STEP} = 10 V , G = +1, CL = 20 pF			0.91		
		To 0.01%, V_S = 40 V, V_{STEP} = 2 V , G = +1, CL = 20 pF			0.48		
	Phase margin	G = +1, R_L = 10kΩ, C_L = 20 pF			56		°
	Overload recovery time	V_{IN} × gain > V_S			300		ns

6.17 Electrical Characteristics: TL07xH (continued)

For $V_S = (V_{CC+}) – (V_{CC–})$ = 4.5 V to 40 V (±2.25 V to ±20 V) at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, $V_{CM} = V_S$ / 2, and $V_{OUT} = V_S$ / 2, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
THD+N	Total harmonic distortion + noise	V_S = 40 V, V_O = 6 V_{RMS}, G = +1, f = 1 kHz			0.00012		%
EMIRR	EMI rejection ratio	f = 1 GHz			53		dB
OUTPUT							
	Voltage output swing from rail	Positive rail headroom	V_S = 40 V, R_L = 10 kΩ		115	210	mV
			V_S = 40 V, R_L = 2 kΩ		520	965	
		Negative rail headroom	V_S = 40 V, R_L = 10 kΩ		105	215	
			V_S = 40 V, R_L = 2 kΩ		500	1030	
I_{SC}	Short-circuit current				±26		mA
C_{LOAD}	Capacitive load drive				300		pF
Z_O	Open-loop output impedance	f = 1 MHz, I_O = 0 A			125		Ω
POWER SUPPLY							
I_Q	Quiescent current per amplifier	I_O = 0 A			937.5	1125	μA
		I_O = 0 A, (TL071H)			960	1156	
		I_O = 0 A	T_A = –40°C to 125°C			1130	
		I_O = 0 A, (TL072H)				1143	
		I_O = 0 A, (TL071H)				1160	
	Turn-On Time	At T_A = 25°C, V_S = 40 V, V_S ramp rate > 0.3 V/μs			60		μs

(1) Max I_B and I_{os} data is specified based on characterization results.

6.18 Electrical Characteristics: TL071C, TL072C, TL074C

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	T_A = 25°C		3	10	mV
			T_A = Full range			13	
α	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	T_A = Full range		18		µV/°C
I_{IO}	Input offset current	$V_O = 0$	T_A = 25°C		5	100	pA
			T_A = Full range			10	nA
I_{IB}	Input bias current (3)	$V_O = 0$	T_A = 25°C		65	200	pA
			T_A = Full range			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	T_A = 25°C	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	T_A = Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10\ V$ $R_L \geq 2\ k\Omega$	T_A = 25°C	25	200		V/mV
			T_A = Full range	15			
B_1	Utility-gain bandwidth	T_A = 25°C			3		MHz
r_I	Input resistance	T_A = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$ $V_O = 0$ $R_S = 50\ \Omega$	T_A = 25°C	70	100		dB
k_{SVR}	Supply voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V $V_O = 0$ $R_S = 50\ \Omega$	T_A = 25°C	70	100		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	T_A = 25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-40. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.19 Electrical Characteristics: TL071AC, TL072AC, TL074AC

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	V_O = 0 R_S = 50 Ω	T_A = 25°C		3	6	mV
			T_A = Full range			7.5	
α	Temperature coefficient of input offset voltage	V_O = 0 R_S = 50 Ω	T_A = Full range		18		μV/°C
I_{IO}	Input offset current	V_O = 0	T_A = 25°C		5	100	pA
			T_A = Full range			2	nA
I_{IB}	Input bias current (3)	V_O = 0	T_A = 25°C		65	200	pA
			T_A = Full range			7	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	R_L= 10 kΩ	T_A = 25°C	±12	±13.5		V
		R_L≥ 10 kΩ	T_A = Full range	±12			
		R_L≥ 2 kΩ		±10			
A_{VD}	Large-signal differential voltage amplification	V_O = ±10 V R_L≥ 2 kΩ	T_A = 25°C	50	200		V/mV
			T_A = Full range	25			
B_1	Utility-gain bandwidth	T_A = 25°C			3		MHz
r_I	Input resistance	T_A = 25°C			10^{12}		Ω
CMRR	Common-mode rejection ratio	V_{IC} = $V_{ICR(min)}$ V_O = 0 R_S = 50 Ω	T_A = 25°C	75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}$ / ΔV_{IO})	V_{CC} = ±9 V to ±15 V V_O = 0 R_S = 50 Ω	T_A = 25°C	80	100		dB
I_{CC}	Supply current (each amplifier)	V_O = 0; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	A_{VD} = 100	T_A = 25°C		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-40. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.20 Electrical Characteristics: TL071BC, TL072BC, TL074BC

$V_{CC\pm} = \pm15$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$		2	3	mV
			T_A = Full range			5	
α	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	T_A = Full range		18		µV/°C
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		5	100	pA
			T_A = Full range			2	nA
I_{IB}	Input bias current (3)	$V_O = 0$	$T_A = 25°C$		65	200	pA
			T_A = Full range			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	$T_A = 25°C$	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	T_A = Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm10$ V $R_L \geq 2\ k\Omega$	$T_A = 25°C$	50	200		V/mV
			T_A = Full range	25			
B_1	Utility-gain bandwidth	$T_A = 25°C$			3		MHz
r_I	Input resistance	$T_A = 25°C$			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$	75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm9$ V to ±15 V $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$	80	100		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25°C$		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25°C$		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) Full range is T_A = 0°C to 70°C.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-40. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.21 Electrical Characteristics: TL071I, TL072I, TL074I

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$		3	6	mV
			T_A = Full range			8	
α	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	T_A = Full range		18		μV/°C
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		5	100	pA
			T_A = Full range			2	nA
I_{IB}	Input bias current (3)	$V_O = 0$	$T_A = 25°C$		65	200	pA
			T_A = Full range			7	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	$T_A = 25°C$	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	T_A = Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10\ V$ $R_L \geq 2\ k\Omega$	$T_A = 25°C$	50	200		V/mV
			T_A = Full range	25			
B_1	Utility-gain bandwidth	$T_A = 25°C$			3		MHz
r_I	Input resistance	$T_A = 25°C$			10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$	75	100		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9\ V$ to $\pm 15\ V$ $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$	80	100		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25°C$		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25°C$		120		dB

(1) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified.
(2) T_A = –40°C to 85°C.
(3) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-40. Pulse techniques must be used that maintain the junction temperature as close to the ambient temperature as possible.

6.22 Electrical Characteristics: TL071M, TL072M

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS (1) (2)		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$		3	6	mV
			T_A = Full range			9	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	T_A = Full range		18		μV/°C
I_{IO}	Input offset current	$V_O = 0$	$T_A = 25°C$		5	100	pA
			T_A = Full range			20	nA
I_{IB}	Input bias current	$V_O = 0$	$T_A = 25°C$		65	200	pA
			T_A = Full range			50	nA
V_{ICR}	Common-mode input voltage range	$T_A = 25°C$		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	$T_A = 25°C$	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	T_A = Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V $R_L \geq 2\ k\Omega$	$T_A = 25°C$	35	200		V/mV
			T_A = Full range	15			
B_1	Unity-gain bandwidth				3		MHz
r_i	Input resistance				10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$, $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$	80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	$V_{CC} = \pm 9$ V to ±15 V $V_O = 0$ $R_S = 50\ \Omega$	$T_A = 25°C$	80	86		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$; no load	$T_A = 25°C$		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	$T_A = 25°C$		120		dB

(1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-40. Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used.

(2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = –55°C to +125°C.

6.23 Electrical Characteristics: TL074M

$V_{CC\pm}$ = ±15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS [1] [2]		MIN	TYP	MAX	UNIT
V_{IO}	Input offset voltage	$V_O = 0$ $R_S = 50\ \Omega$	T_A = 25°C		3	9	mV
			T_A = Full range			15	
α_{VIO}	Temperature coefficient of input offset voltage	$V_O = 0$, $R_S = 50\ \Omega$	T_A = Full range		18		µV/°C
I_{IO}	Input offset current	$V_O = 0$	T_A = 25°C		5	100	pA
			T_A = Full range			20	nA
I_{IB}	Input bias current	$V_O = 0$	T_A = 25°C		65	200	pA
			T_A = Full range			20	nA
V_{ICR}	Common-mode input voltage range	T_A = 25°C		±11	–12 to 15		V
V_{OM}	Maximum peak output voltage swing	$R_L = 10\ k\Omega$	T_A = 25°C	±12	±13.5		V
		$R_L \geq 10\ k\Omega$	T_A = Full range	±12			
		$R_L \geq 2\ k\Omega$		±10			
A_{VD}	Large-signal differential voltage amplification	$V_O = \pm 10$ V $R_L \geq 2\ k\Omega$	T_A = 25°C	35	200		V/mV
			T_A = Full range	15			
B_1	Unity-gain bandwidth				3		MHz
r_i	Input resistance				10^{12}		Ω
CMRR	Common-mode rejection ratio	$V_{IC} = V_{ICR(min)}$ $V_O = 0$ $R_S = 50\ \Omega$	T_A = 25°C	80	86		dB
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{CC\pm}/\Delta V_{IO}$)	V_{CC} = ±9 V to ±15 V $V_O = 0$ $R_S = 50\ \Omega$	T_A = 25°C	80	86		dB
I_{CC}	Supply current (each amplifier)	$V_O = 0$; no load	T_A = 25°C		1.4	2.5	mA
V_{O1} / V_{O2}	Crosstalk attenuation	$A_{VD} = 100$	T_A = 25°C		120		dB

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(1) Input bias currents of an FET-input operational amplifier are normal junction reverse currents, which are temperature sensitive, as shown in Figure 6-40. Pulse techniques that maintain the junction temperature as close to the ambient temperature as possible must be used .

(2) All characteristics are measured under open-loop conditions with zero common-mode voltage, unless otherwise specified. Full range is T_A = –55°C to +125°C.

6.24 Switching Characteristics: TL07xM

$V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V C_L = 100 pF	R_L = 2 kΩ See Figure 7-1	5	13		V/μs
t_r	Rise-time overshoot factor	V_I = 20 V C_L = 100 pF	R_L = 2 kΩ See Figure 7-1		0.1		μs
					20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 20 Ω	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V R_L ≥ 2 kΩ f = 1 kHz	A_{VD} = 1 RS ≤ 1 kΩ		0.003%		

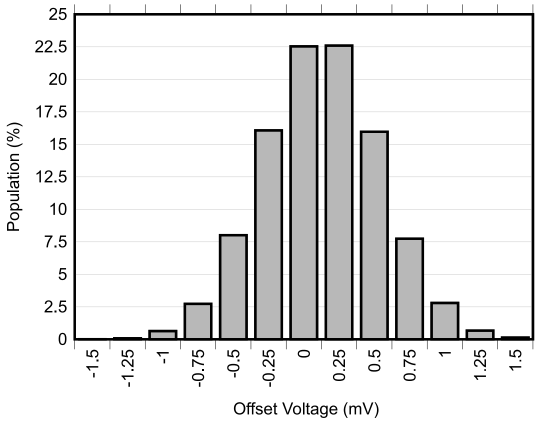
6.25 Switching Characteristics: TL07xC, TL07xAC, TL07xBC, TL07xI

$V_{CC\pm}$ = ±15 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	V_I = 10 V C_L = 100 pF	R_L = 2 kΩ See Figure 7-1	8	13		V/μs
t_r	Rise-time overshoot factor	V_I = 20 V C_L = 100 pF	R_L = 2 kΩ See Figure 7-1		0.1		μs
					20%		
V_n	Equivalent input noise voltage	R_S = 20 Ω	f = 1 kHz		18		nV/√Hz
			f = 10 Hz to 10 kHz		4		μV
I_n	Equivalent input noise current	R_S = 20 Ω	f = 1 kHz		0.01		pA/√Hz
THD	Total harmonic distortion	$V_I$rms = 6 V R_L ≥ 2 kΩ f = 1 kHz	A_{VD} = 1 RS ≤ 1 kΩ		0.003%		

6.26 Typical Characteristics: TL07xH

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



T_A = 25°C

Figure 6-1. Offset Voltage Production Distribution

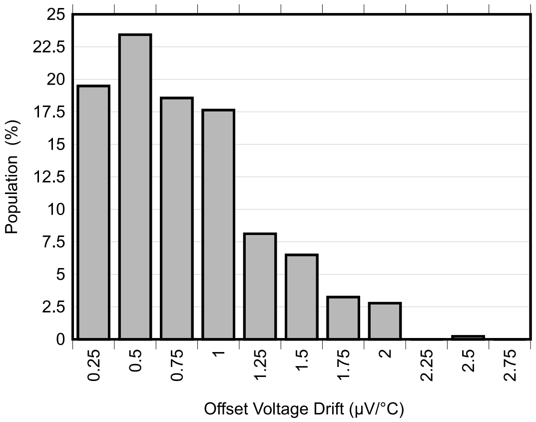
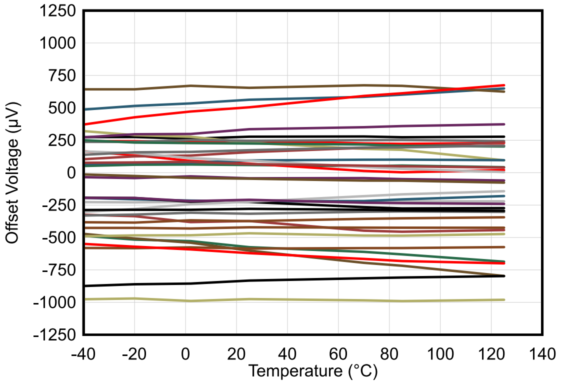
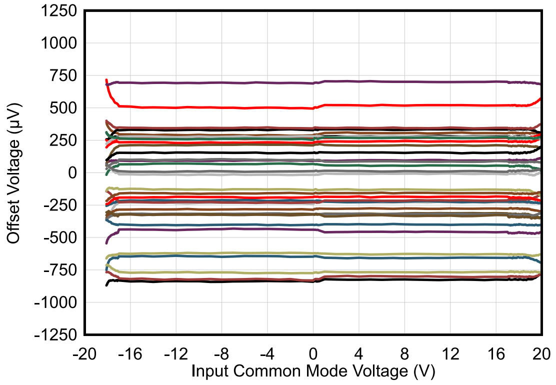


Figure 6-2. Offset Voltage Drift Distribution



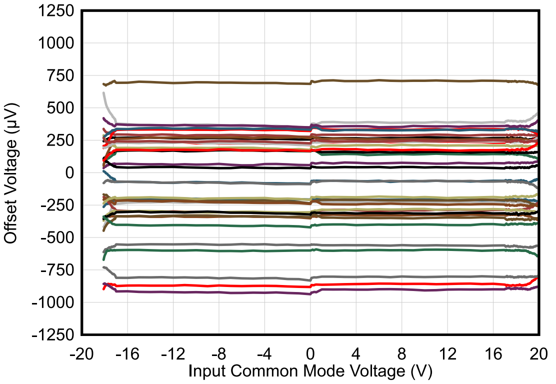
V_{CM} = V_S / 2

Figure 6-3. Offset Voltage vs Temperature



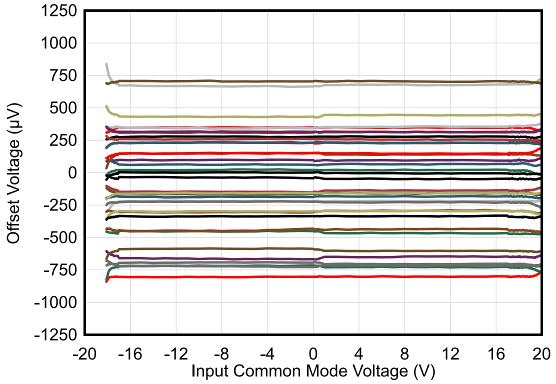
T_A = 25°C

Figure 6-4. Offset Voltage vs Common-Mode Voltage



T_A = 125°C

Figure 6-5. Offset Voltage vs Common-Mode Voltage



T_A = –40°C

Figure 6-6. Offset Voltage vs Common-Mode Voltage

6.26 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

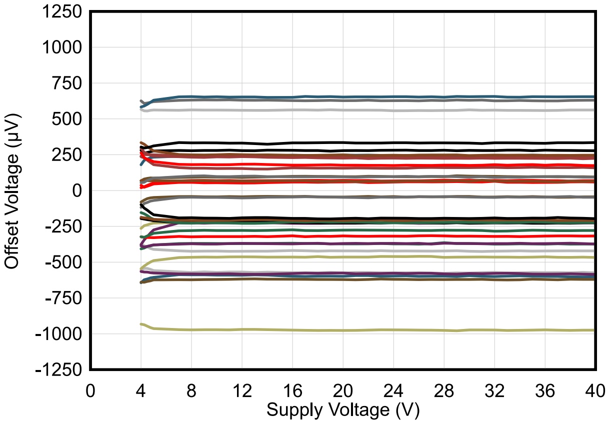


Figure 6-7. Offset Voltage vs Power Supply

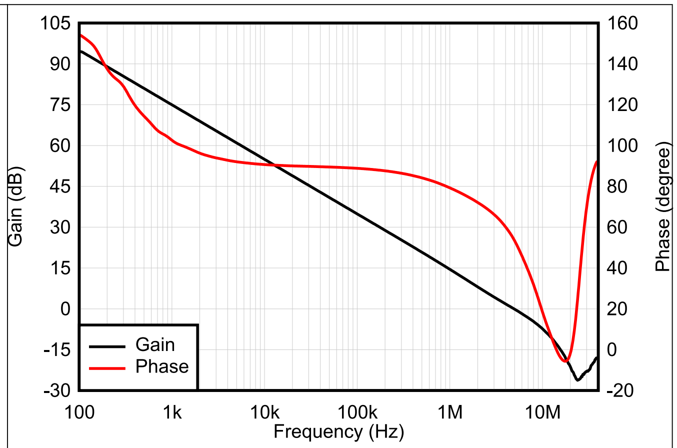


Figure 6-8. Open-Loop Gain and Phase vs Frequency

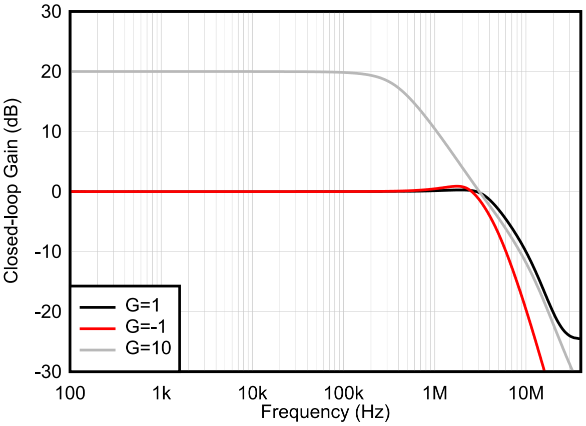


Figure 6-9. Closed-Loop Gain vs Frequency

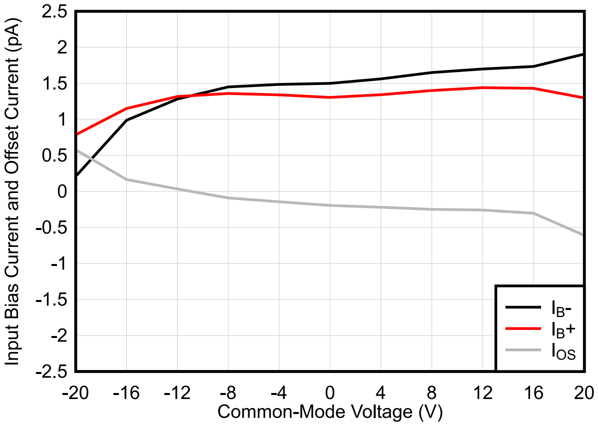


Figure 6-10. Input Bias Current vs Common-Mode Voltage

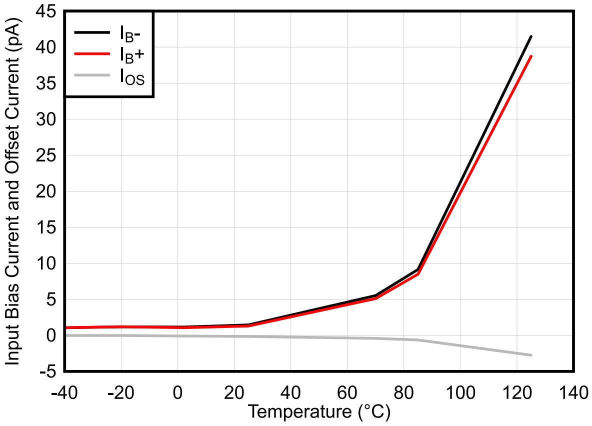


Figure 6-11. Input Bias Current vs Temperature

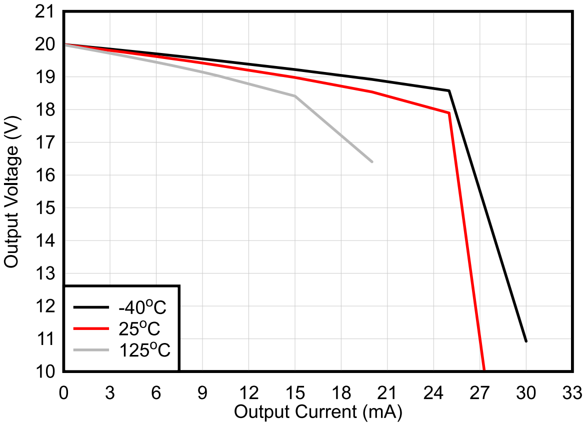


Figure 6-12. Output Voltage Swing vs Output Current (Sourcing)

6.26 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

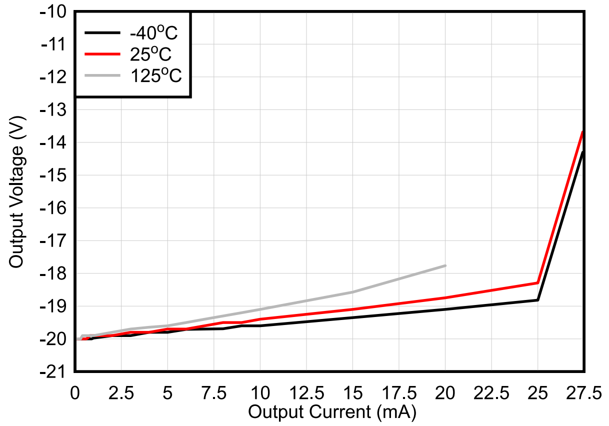


Figure 6-13. Output Voltage Swing vs Output Current (Sinking)

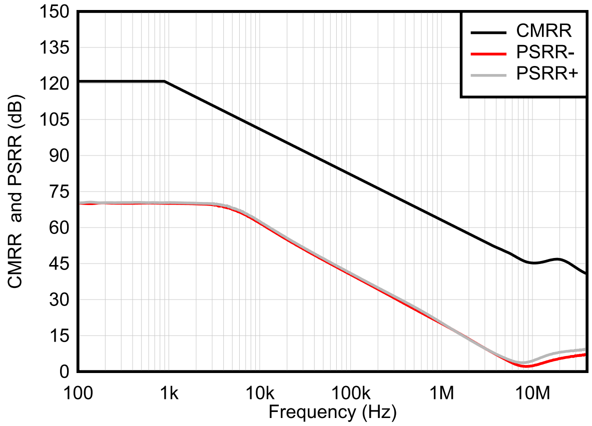
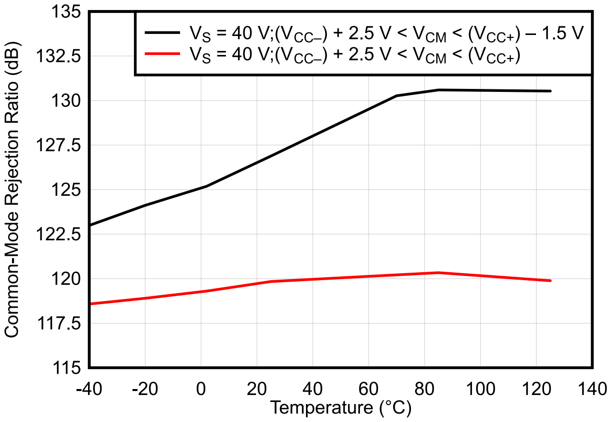
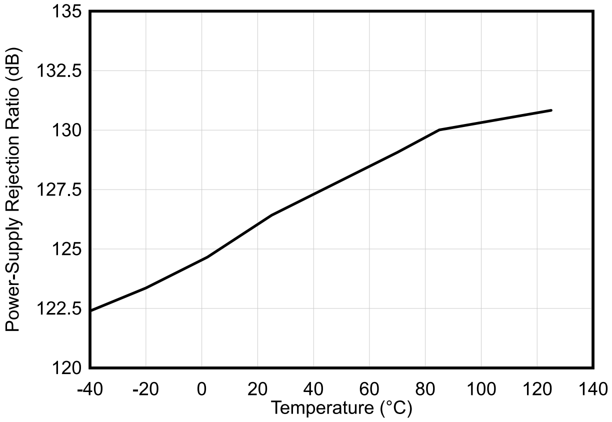


Figure 6-14. CMRR and PSRR vs Frequency



f = 0 Hz

Figure 6-15. CMRR vs Temperature (dB)



f = 0 Hz

Figure 6-16. PSRR vs Temperature (dB)

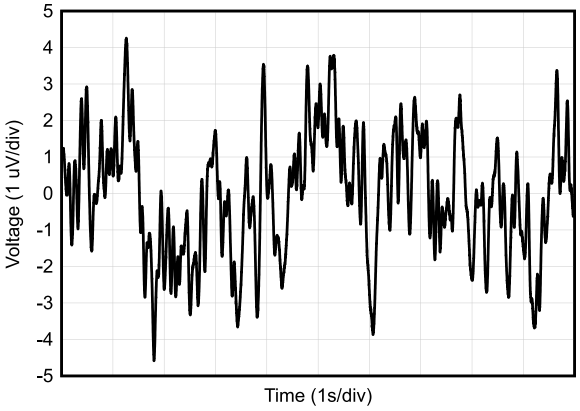


Figure 6-17. 0.1-Hz to 10-Hz Noise

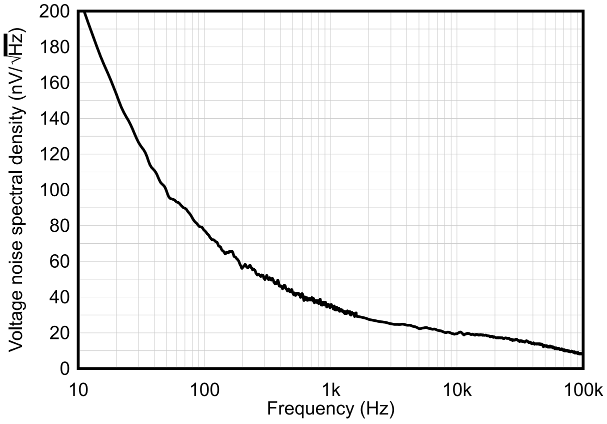
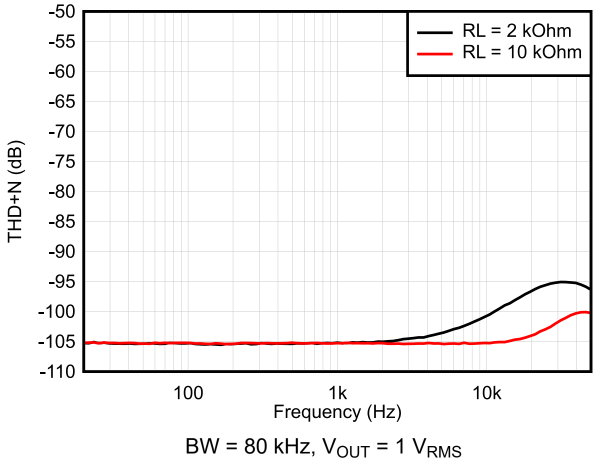


Figure 6-18. Input Voltage Noise Spectral Density vs Frequency

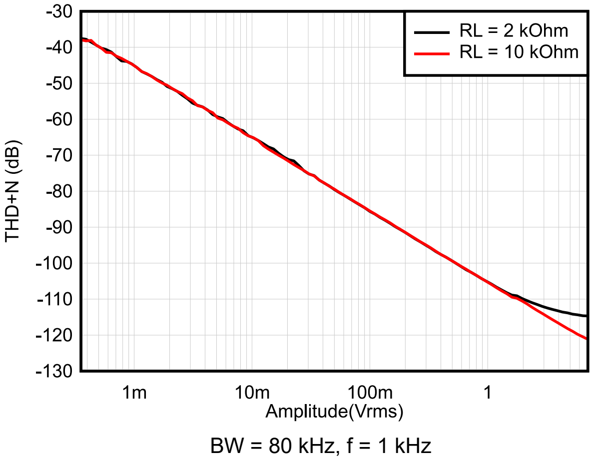
6.26 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



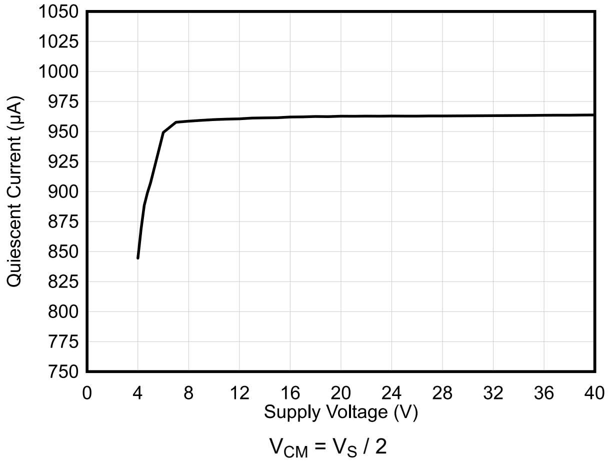
BW = 80 kHz, V_{OUT} = 1 V_{RMS}

Figure 6-19. THD+N Ratio vs Frequency



BW = 80 kHz, f = 1 kHz

Figure 6-20. THD+N vs Output Amplitude



V_{CM} = V_S / 2

Figure 6-21. Quiescent Current vs Supply Voltage

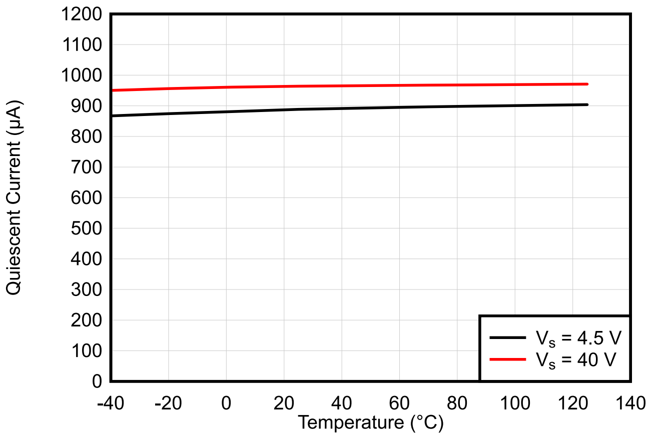


Figure 6-22. Quiescent Current vs Temperature

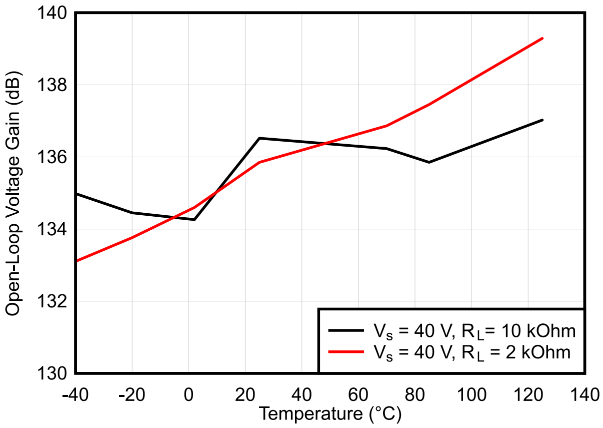


Figure 6-23. Open-Loop Voltage Gain vs Temperature (dB)

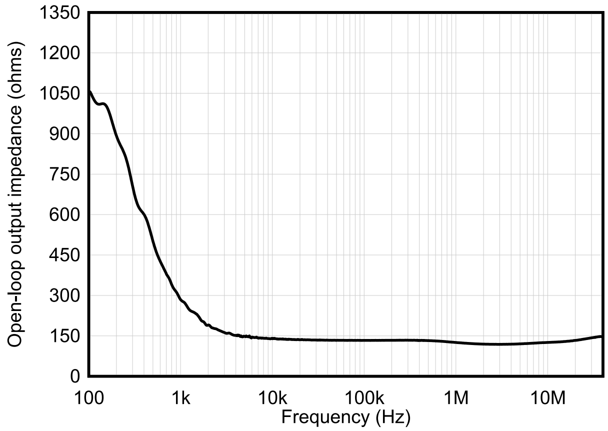
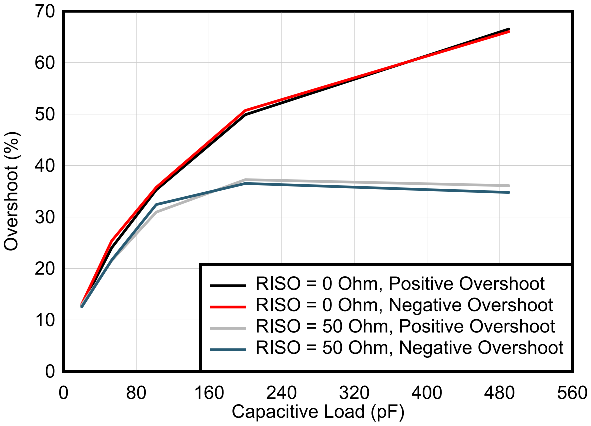


Figure 6-24. Open-Loop Output Impedance vs Frequency

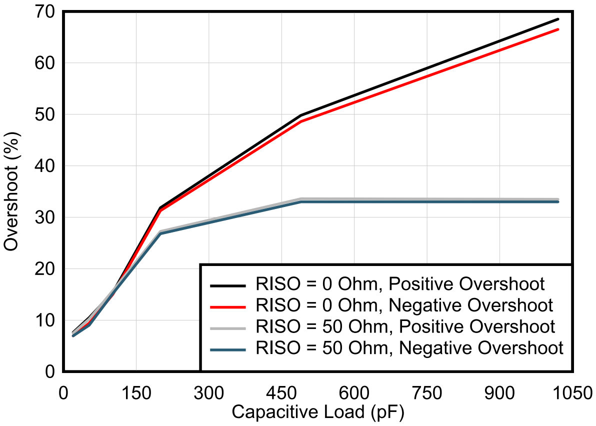
6.26 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



G = –1, 25-mV output step

Figure 6-25. Small-Signal Overshoot vs Capacitive Load



G = 1, 10-mV output step

Figure 6-26. Small-Signal Overshoot vs Capacitive Load

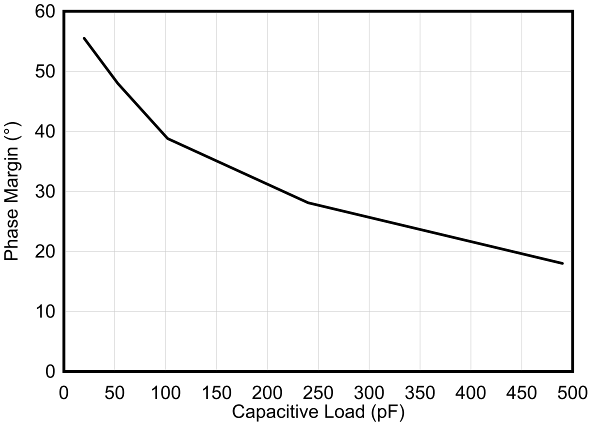
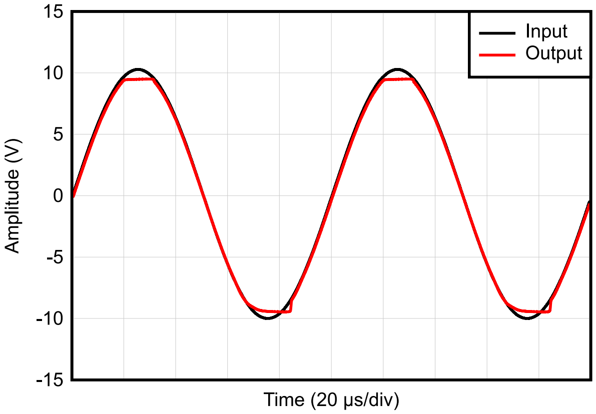
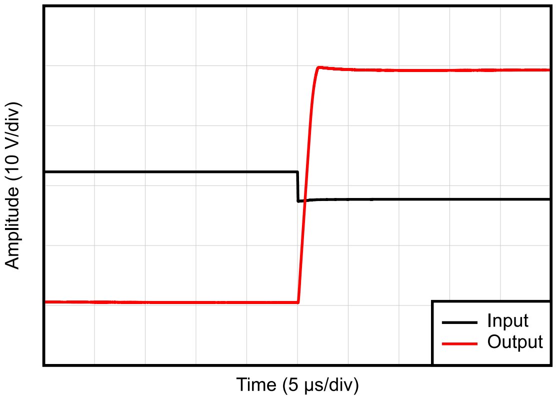


Figure 6-27. Phase Margin vs Capacitive Load



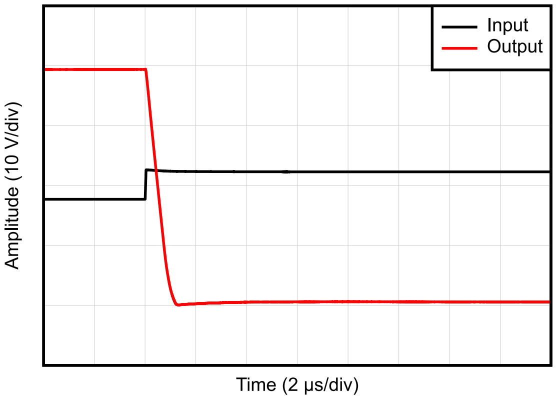
V_S = ±10 V, V_{IN} = V_{OUT}

Figure 6-28. No Phase Reversal



G = –10

Figure 6-29. Positive Overload Recovery

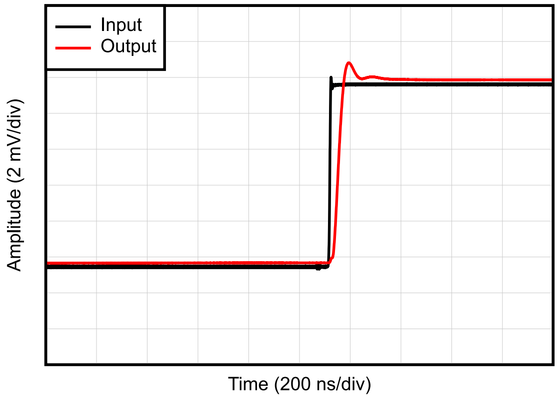


G = –10

Figure 6-30. Negative Overload Recovery

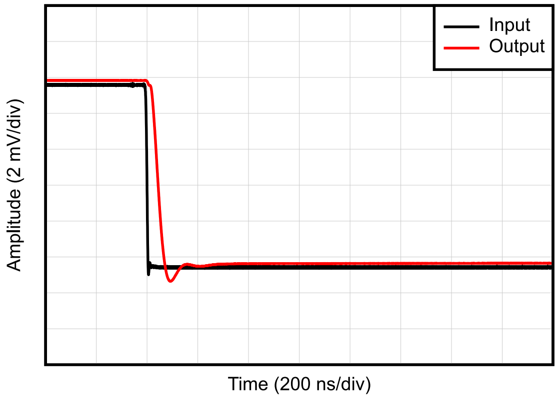
6.26 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)



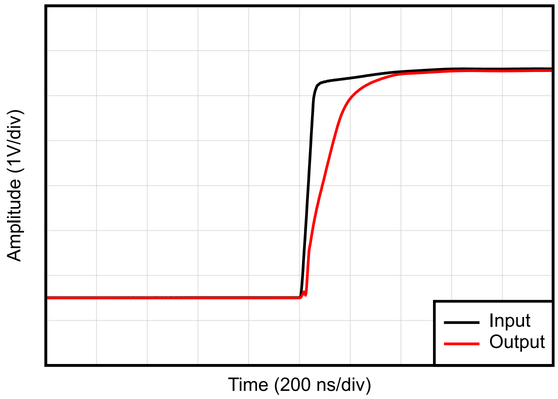
C_L = 20 pF, G = 1, 10-mV step response

Figure 6-31. Small-Signal Step Response, Rising



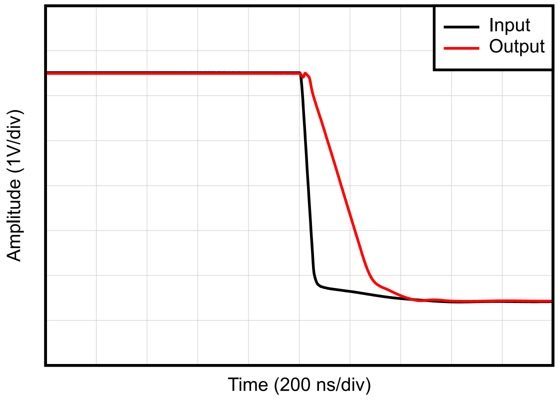
C_L = 20 pF, G = 1, 10-mV step response

Figure 6-32. Small-Signal Step Response, Falling



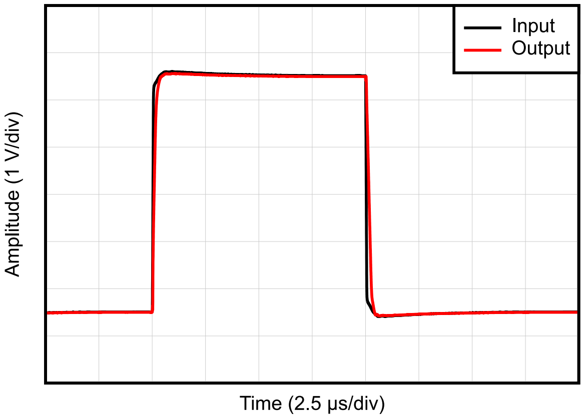
C_L = 20 pF, G = 1

Figure 6-33. Large-Signal Step Response (Rising)



C_L = 20 pF, G = 1

Figure 6-34. Large-Signal Step Response (Falling)



C_L = 20 pF, G = 1

Figure 6-35. Large-Signal Step Response

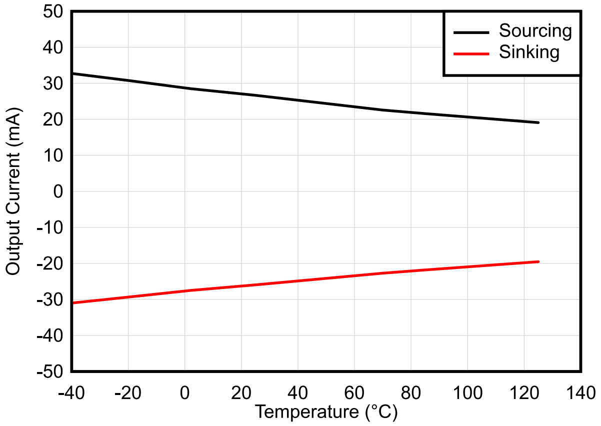


Figure 6-36. Short-Circuit Current vs Temperature

6.26 Typical Characteristics: TL07xH (continued)

at T_A = 25°C, V_S = 40 V (±20 V), V_{CM} = V_S / 2, R_{LOAD} = 10 kΩ connected to V_S / 2, and C_L = 20 pF (unless otherwise noted)

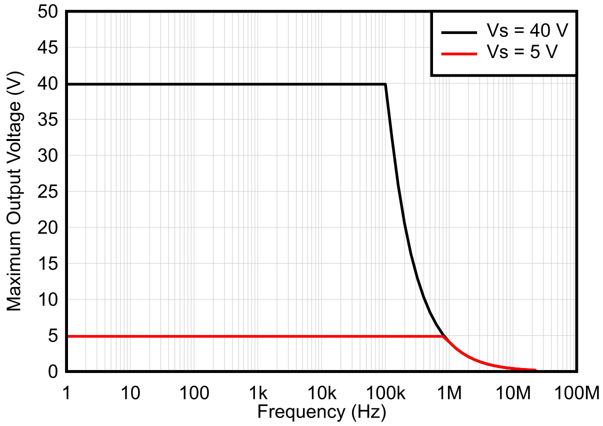


Figure 6-37. Maximum Output Voltage vs Frequency

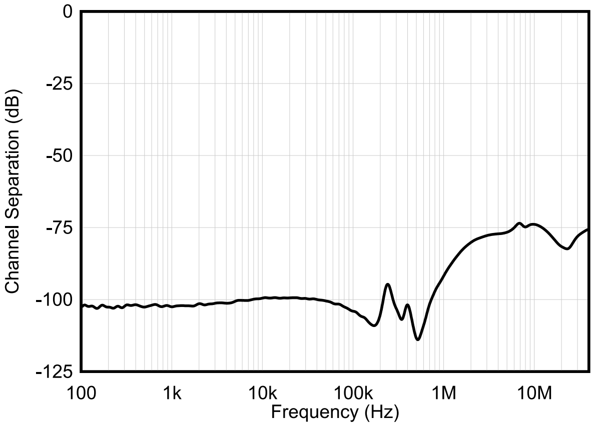


Figure 6-38. Channel Separation vs Frequency

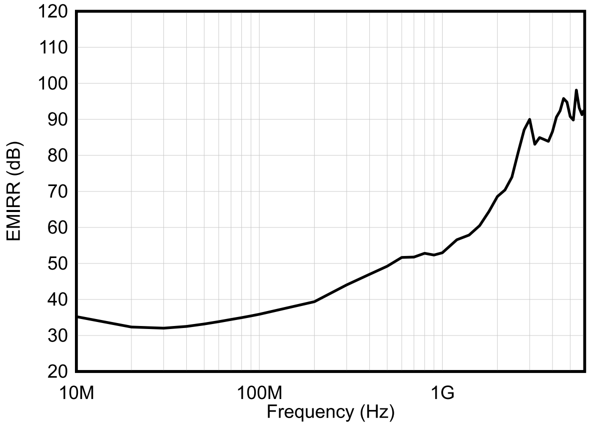


Figure 6-39. EMIRR (Electromagnetic Interference Rejection Ratio) vs Frequency

6.27 Typical Characteristics: All Devices Except TL07xH

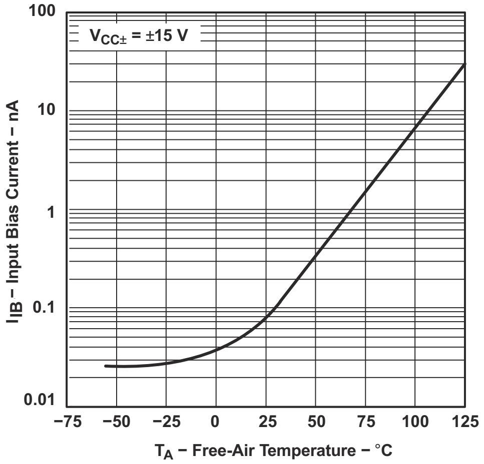


Figure 6-40. Input Bias Current vs Free-Air Temperature

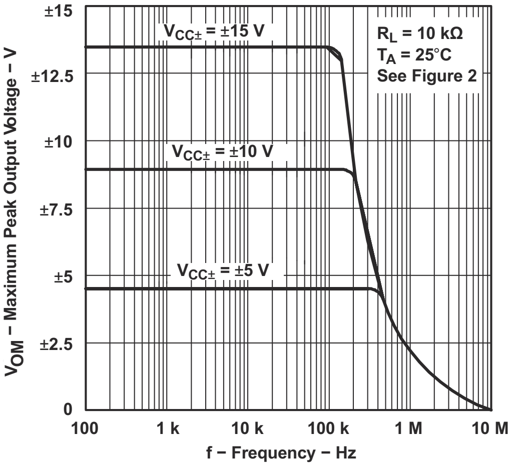


Figure 6-41. Maximum Peak Output Voltage vs Frequency

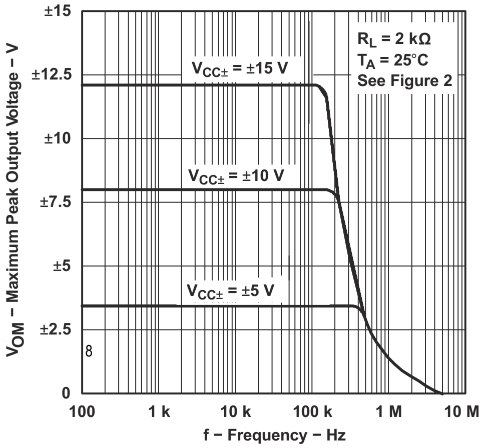


Figure 6-42. Maximum Peak Output Voltage vs Frequency

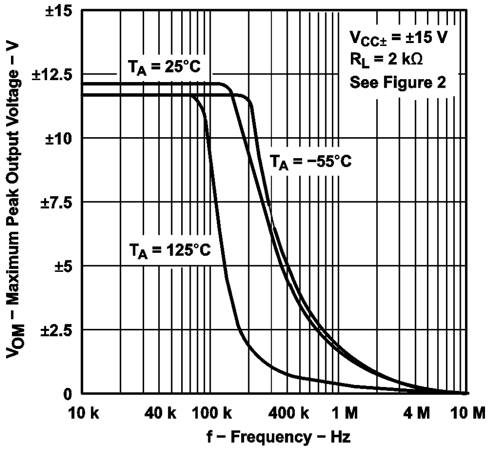


Figure 6-43. Maximum Peak Output Voltage vs Frequency

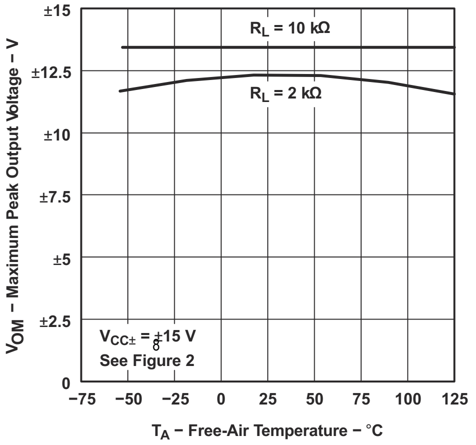


Figure 6-44. Maximum Peak Output Voltage vs Free-Air Temperature

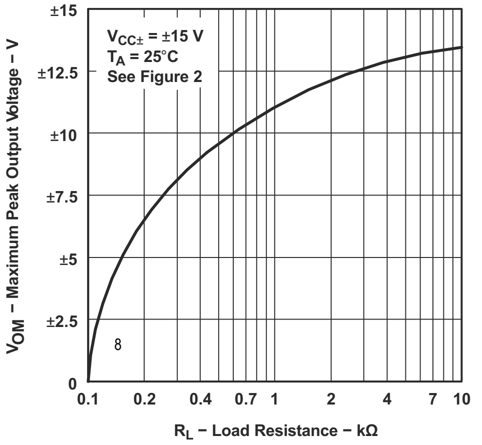


Figure 6-45. Maximum Peak Output Voltage vs Load Resistance

6.27 Typical Characteristics: All Devices Except TL07xH (continued)

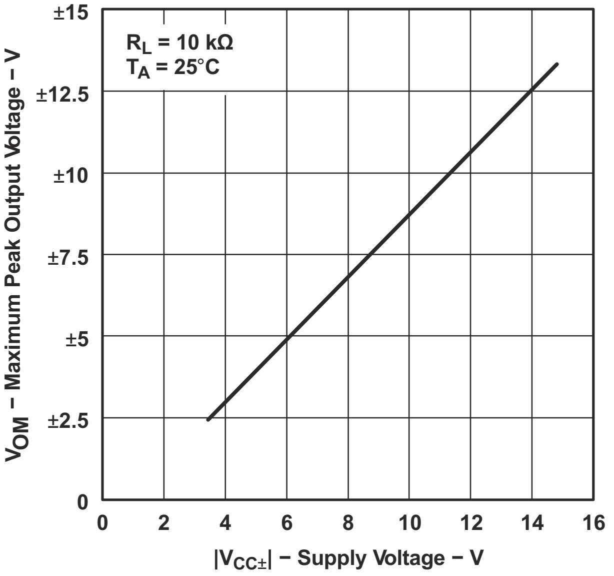


Figure 6-46. Maximum Peak Output Voltage vs Supply Voltage

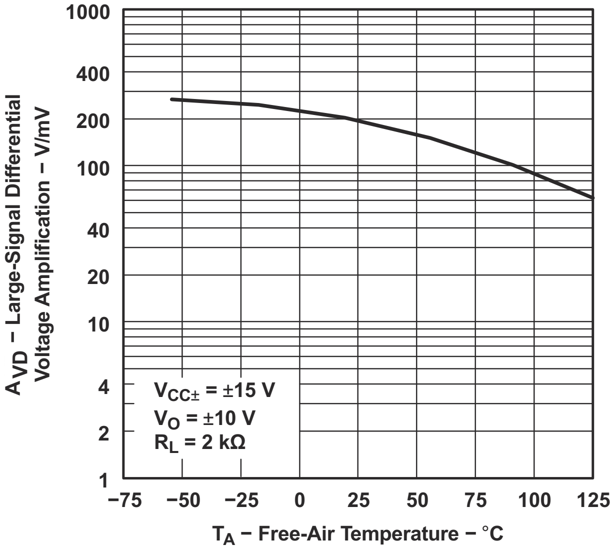


Figure 6-47. Large-Signal Differential Voltage Amplification vs Free-Air Temperature

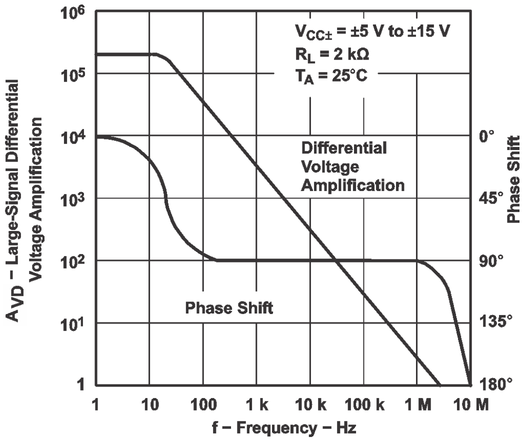


Figure 6-48. Large-Signal Differential Voltage Amplification and Phase Shift vs Frequency

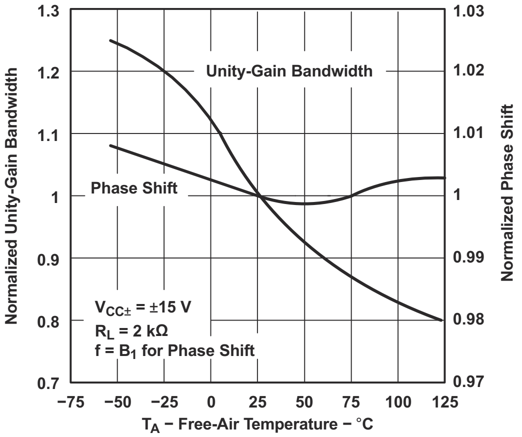


Figure 6-49. Normalized Unity-Gain Bandwidth and Phase Shift vs Free-Air Temperature

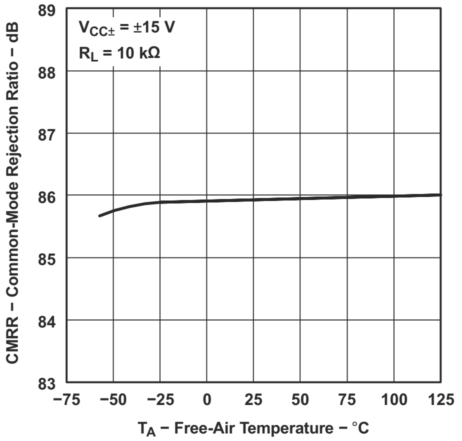


Figure 6-50. Common-Mode Rejection Ratio vs Free-Air Temperature

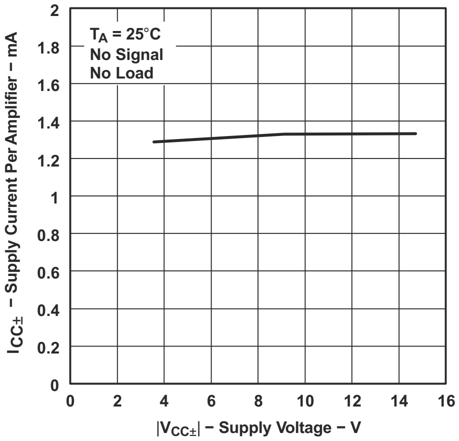


Figure 6-51. Supply Current Per Amplifier vs Supply Voltage

6.27 Typical Characteristics: All Devices Except TL07xH (continued)

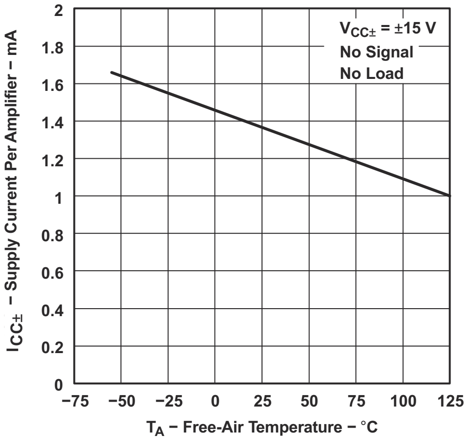


Figure 6-52. Supply Current Per Amplifier vs Free-Air Temperature

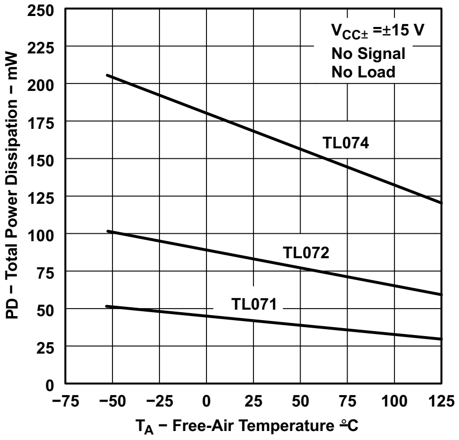


Figure 6-53. Total Power Dissipation vs Free-Air Temperature

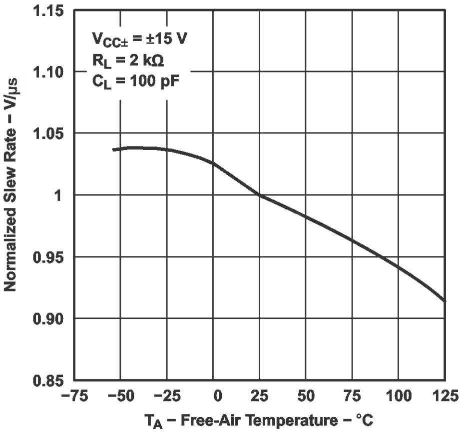


Figure 6-54. Normalized Slew Rate vs Free-Air Temperature

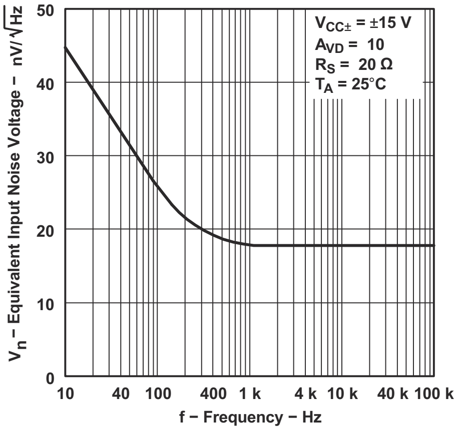


Figure 6-55. Equivalent Input Noise Voltage vs Frequency

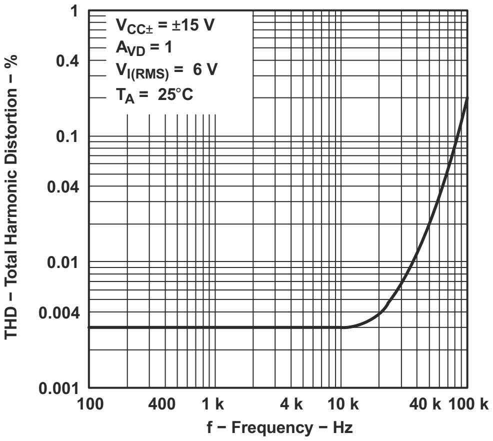


Figure 6-56. Total Harmonic Distortion vs Frequency

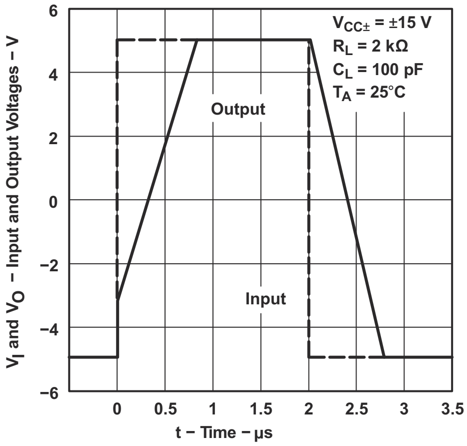


Figure 6-57. Voltage-Follower Large-Signal Pulse Response

6.27 Typical Characteristics: All Devices Except TL07xH (continued)

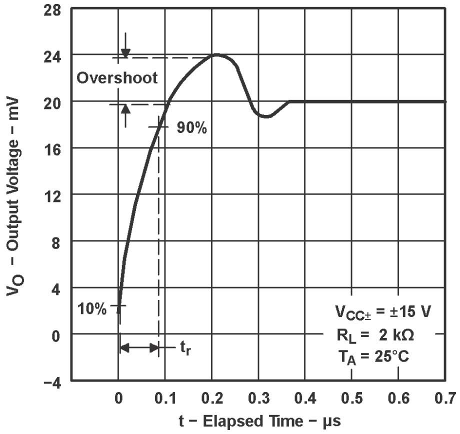


Figure 6-58. Output Voltage vs Elapsed Time

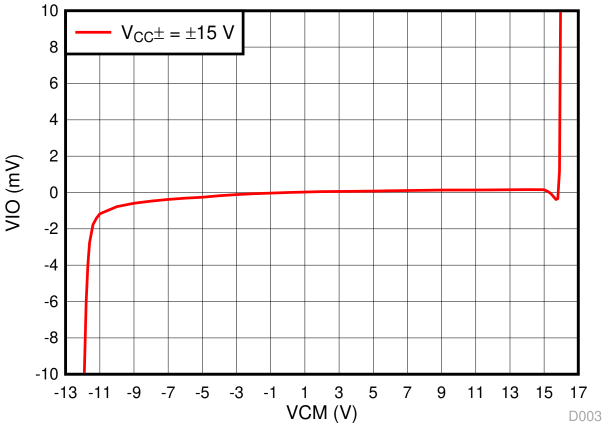


Figure 6-59. V_{IO} vs V_{CM}

7 Parameter Measurement Information

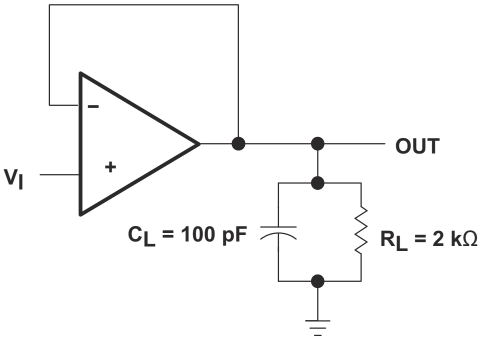


Figure 7-1. Unity-Gain Amplifier

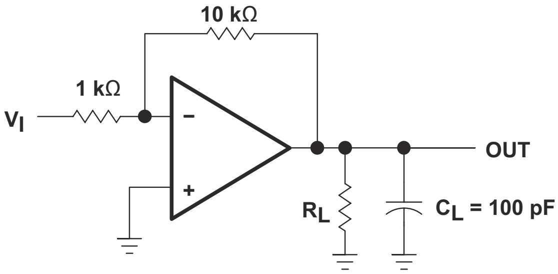


Figure 7-2. Gain-of-10 Inverting Amplifier

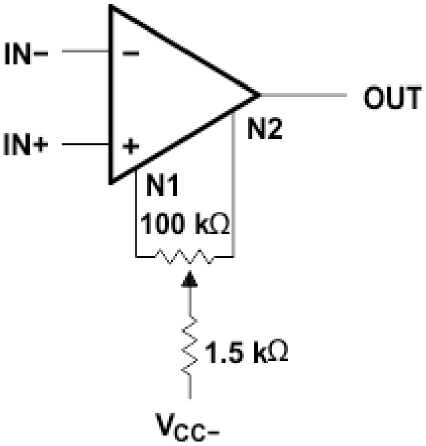


Figure 7-3. Input Offset-Voltage Null Circuit

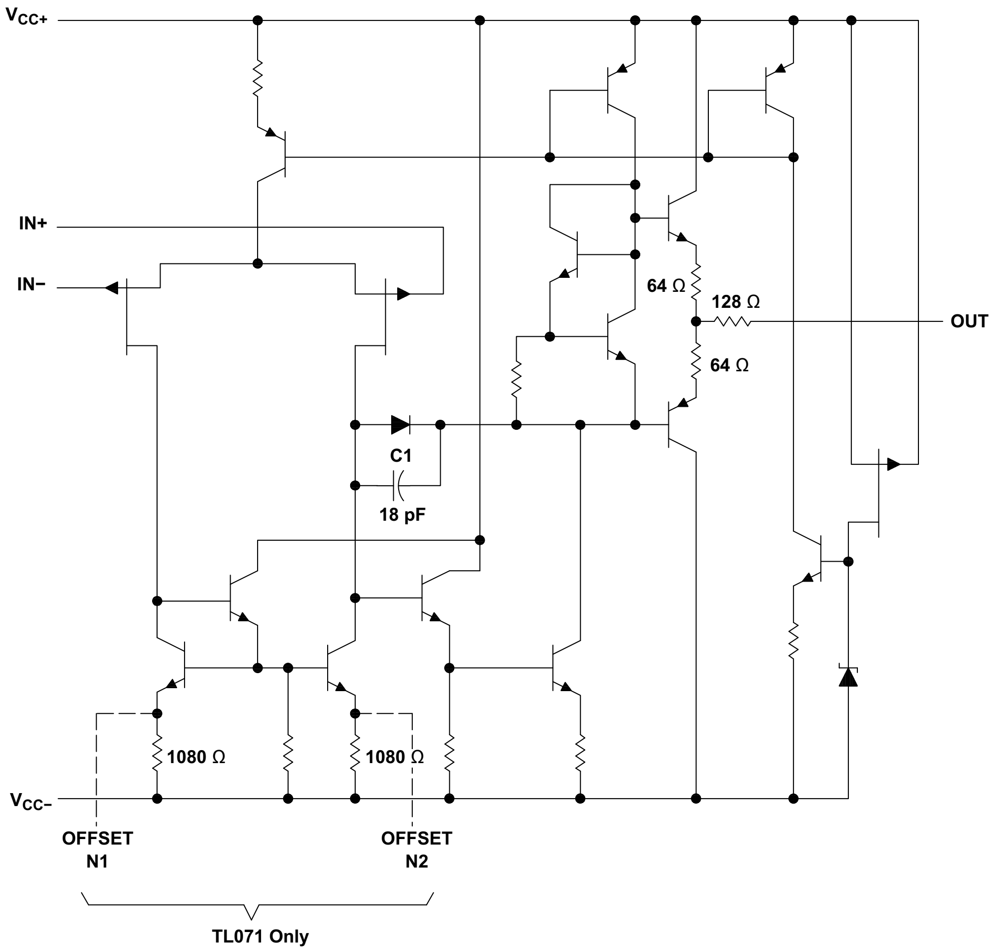
8 Detailed Description

8.1 Overview

The TL07xH (TL071H, TL072H, and TL074H) family of devices are the next-generation versions of the industry-standard TL07x (TL071, TL072, and TL074) devices. These devices provide outstanding value for cost-sensitive applications, with features including low offset (1 mV, typ), high slew rate (25 V/μs, typ), and common-mode input to the positive supply. High ESD (1.5 kV, HBM), integrated EMI and RF filters, and operation across the full –40°C to 125°C enable the TL07xH devices to be used in the most rugged and demanding applications.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from −40°C to +85°C. The M-suffix devices are characterized for operation over the full military temperature range of −55°C to +125°C.

8.2 Functional Block Diagram



All component values shown are nominal.

COMPONENT COUNT†			
COMPONENT TYPE	TL071	TL072	TL074
Resistors	11	22	44
Transistors	14	28	56
JFET	2	4	6
Diodes	1	2	4
Capacitors	1	2	4
epi-FET	1	2	4

† Includes bias and trim circuitry

8.3 Feature Description

The TL07xH family of devices improve many specifications as compared to the industry-standard TL07x family. Several comparisons of key specifications between these families are included below to show the advantages of the TL07xH family.

8.3.1 Total Harmonic Distortion

Harmonic distortions to an audio signal are created by electronic components in a circuit. Total harmonic distortion (THD) is a measure of harmonic distortions accumulated by a signal in an audio system. These devices have a very low THD of 0.003% meaning that the TL07x device adds little harmonic distortion when used in audio signal applications.

8.3.2 Slew Rate

The slew rate is the rate at which an operational amplifier can change the output when there is a change on the input. These devices have a 13-V/µs slew rate.

8.4 Device Functional Modes

These devices are powered on when the supply is connected. These devices can be operated as a single-supply operational amplifier or dual-supply amplifier depending on the application.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

A typical application for an operational amplifier is an inverting amplifier. This amplifier takes a positive voltage on the input, and makes the voltage a negative voltage. In the same manner, the amplifier makes negative voltages positive.

9.2 Typical Application

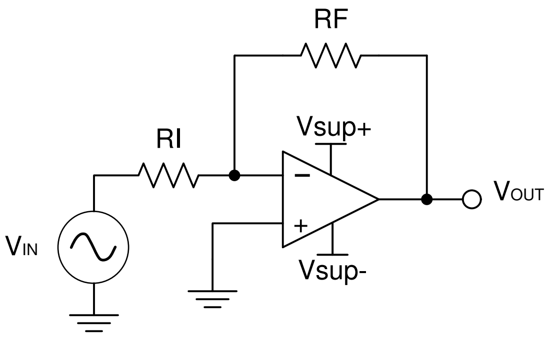


Figure 9-1. Inverting Amplifier

9.2.1 Design Requirements

The supply voltage must be selected so the supply voltage is larger than the input voltage range and output range. For instance, this application scales a signal of ±0.5 V to ±1.8 V. Setting the supply at ±12 V is sufficient to accommodate this application.

9.2.2 Detailed Design Procedure

$$V_o = (V_i + V_{io})*\left(1 + \frac{1M\Omega}{1k\Omega}\right) \quad (1)$$

Determine the gain required by the inverting amplifier:

$$A_V = \frac{VOUT}{VIN} \quad (2)$$

$$A_V = \frac{1.8}{-0.5} = -3.6 \quad (3)$$

Once the desired gain is determined, select a value for RI or RF. Selecting a value in the kilohm range is desirable because the amplifier circuit uses currents in the milliamp range. This ensures the part does not draw too much current. This example uses 10 kΩ for RI which means 36 kΩ is used for RF. This is determined by Equation 4.

$$A_V = -\frac{RF}{RI} \quad (4)$$

9.2.3 Application Curve

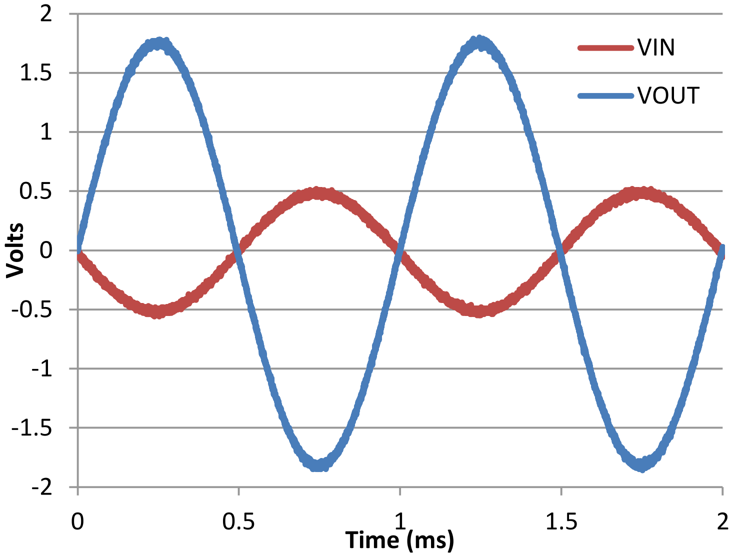


Figure 9-2. Input and Output Voltages of the Inverting Amplifier

9.3 Unity Gain Buffer

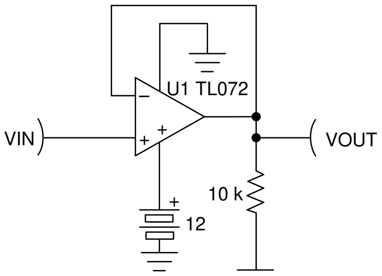


Figure 9-3. Single-Supply Unity Gain Amplifier

9.3.1 Design Requirements

- V_{CC} must be within valid range per Section 6.6. This example uses a value of 12 V for V_{CC}.
- Input voltage must be within the recommended common-mode range, as shown in Section 6.6. The valid common-mode range is 4 V to 12 V (V_{CC-} + 4 V to V_{CC+}).
- Output is limited by output range, which is typically 1.5 V to 10.5 V, or V_{CC-} + 1.5 V to V_{CC+} – 1.5 V.

9.3.2 Detailed Design Procedure

- Avoid input voltage values below 1 V to prevent phase reversal where output goes high.
- Avoid input values below 4 V to prevent degraded V_{IO} that results in an apparent gain greater than 1. This may cause instability in some second-order filter designs.

9.3.3 Application Curves

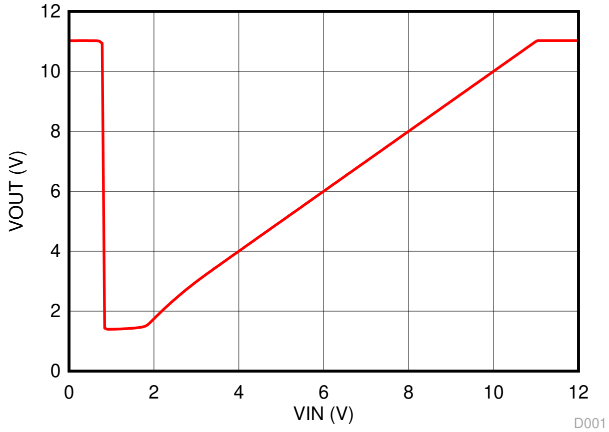


Figure 9-4. Output Voltage vs Input Voltage

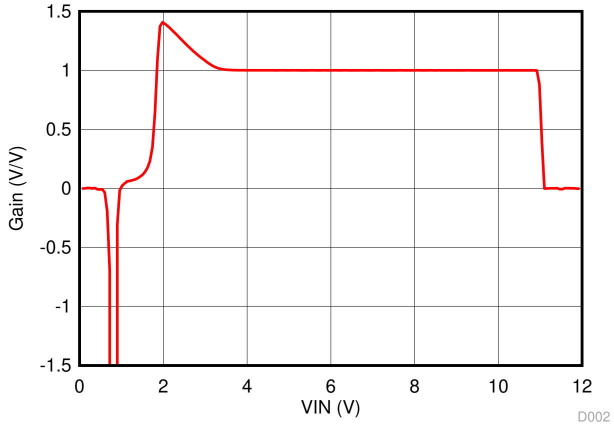


Figure 9-5. Gain vs Input Voltage

9.4 System Examples

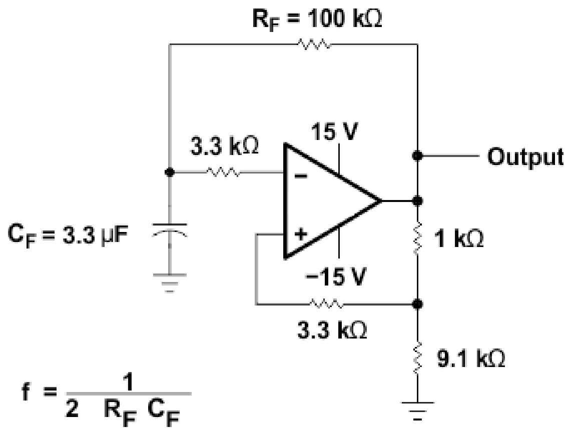


Figure 9-6. 0.5-Hz Square-Wave Oscillator

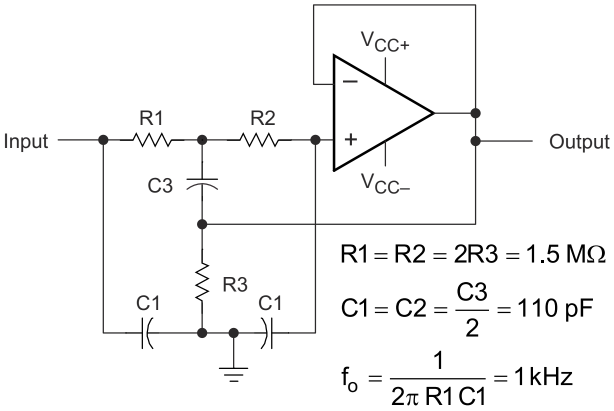


Figure 9-7. High-Q Notch Filter

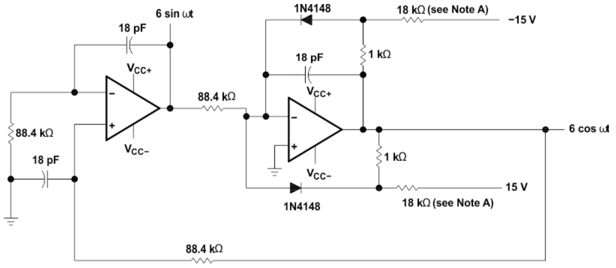


Figure 9-8. 100-kHz Quadrature Oscillator

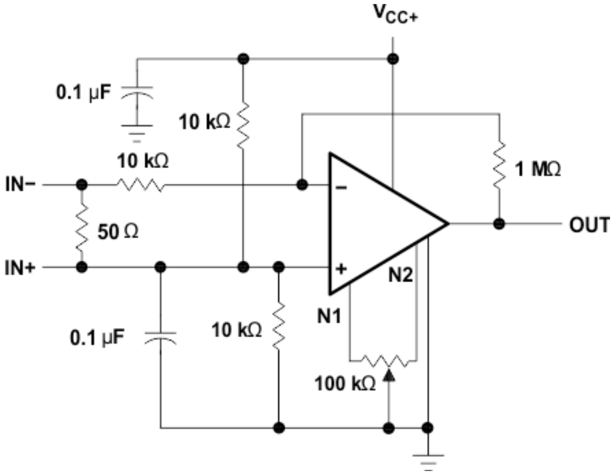


Figure 9-9. AC Amplifier

10 Power Supply Recommendations

CAUTION

Supply voltages larger than 36 V for a single-supply or outside the range of ±18 V for a dual-supply can permanently damage the device (see Section 6.2).

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see Section 11.

11 Layout

11.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as the operational amplifier. Bypass capacitors are used to reduce the coupled noise by providing low impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V_{CC+} to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If it is not possible to keep them separate, it is much better to cross the sensitive trace perpendicular as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance, as shown in Section 11.2.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

11.2 Layout Example

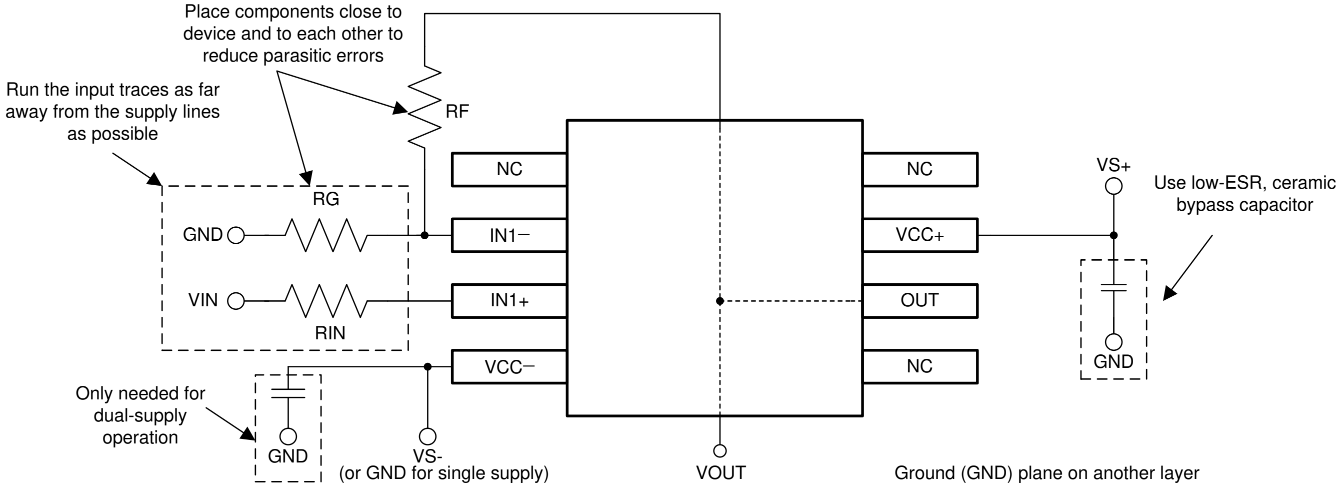


Figure 11-1. Operational Amplifier Board Layout for Noninverting Configuration

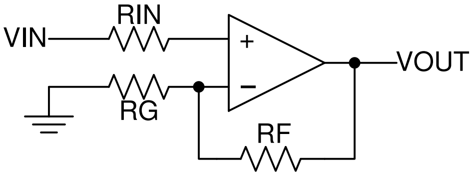


Figure 11-2. Operational Amplifier Schematic for Noninverting Configuration

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
81023052A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
8102305HA	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
8102305PA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
81023062A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
8102306CA	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
8102306DA	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples
JM38510/11905BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
M38510/11905BPA	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510 /11905BPA	Samples
TL071ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	
TL071ACDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	
TL071ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071AC	Samples
TL071ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071ACP	Samples
TL071BCD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	
TL071BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	071BC	Samples
TL071BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071BCP	Samples
TL071CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	
TL071CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL071C	Samples
TL071CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL071CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL071CP	Samples
TL071CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T071	Samples
TL071HIDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T71V	Samples
TL071HIDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	1IO	Samples
TL071HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL071D	Samples
TL071ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	
TL071IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL071I	Samples
TL071IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL071IP	Samples
TL072ACD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	
TL072ACDE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	
TL072ACDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072AC	Samples
TL072ACP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072ACPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072ACP	Samples
TL072BCD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDE4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDG4	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	072BC	Samples
TL072BCDRG4	ACTIVE	SOIC	D	8	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL072BCP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072BCP	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072BCPE4	ACTIVE	PDIP	P	8	50	TBD	Call TI	Call TI	0 to 70		Samples
TL072CD	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	
TL072CDE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	
TL072CDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	
TL072CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL072C	Samples
TL072CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL072CP	Samples
TL072CPS	ACTIVE	SO	PS	8	80	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPSRE4	ACTIVE	SO	PS	8	2000	TBD	Call TI	Call TI	0 to 70		Samples
TL072CPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWRE4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072CPWRG4	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T072	Samples
TL072HIDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	O72F	Samples
TL072HIDR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL072D	Samples
TL072HIPWR	ACTIVE	TSSOP	PW	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	072HPW	Samples
TL072ID	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	
TL072IDE4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	
TL072IDG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	
TL072IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL072IDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL072I	Samples
TL072IP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072IPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL072IP	Samples
TL072MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023052A TL072MFKB	Samples
TL072MJG	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL072MJG	Samples
TL072MJGB	ACTIVE	CDIP	JG	8	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305PA TL072M	Samples
TL072MUB	ACTIVE	CFP	U	10	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102305HA TL072M	Samples
TL074ACD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074AC	Samples
TL074ACDRG4	ACTIVE	SOIC	D	14	2500	TBD	Call TI	Call TI	0 to 70		Samples
TL074ACN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074ACN	Samples
TL074ACNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074A	Samples
TL074BCD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074BCDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074BC	Samples
TL074BCN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074BCNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074BCN	Samples
TL074CD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074C	Samples
TL074CN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNE4	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	TL074CN	Samples
TL074CNSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TL074	Samples
TL074CNSRG4	ACTIVE	SO	NS	14	2000	TBD	Call TI	Call TI	0 to 70		Samples
TL074CPW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRE4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074CPWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	T074	Samples
TL074HIDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074HID	Samples
TL074HIDYYR	ACTIVE	SOT-23-THIN	DYY	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T074HDYY	Samples
TL074HIPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL074PW	Samples
TL074ID	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDE4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TL074IDG4	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRE4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IDRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	TL074I	Samples
TL074IN	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	TL074IN	Samples
TL074MFK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MFK	Samples
TL074MFKB	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	81023062A TL074MFKB	Samples
TL074MJ	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	TL074MJ	Samples
TL074MJB	ACTIVE	CDIP	J	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306CA TL074MJB	Samples
TL074MWB	ACTIVE	CFP	W	14	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8102306DA TL074MWB	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TL072, TL072M, TL074, TL074M :

- Catalog : TL072, TL074

- Enhanced Product : TL072-EP, TL072-EP, TL074-EP, TL074-EP

- Military : TL072M, TL074M

NOTE: Qualified Version Definitions:

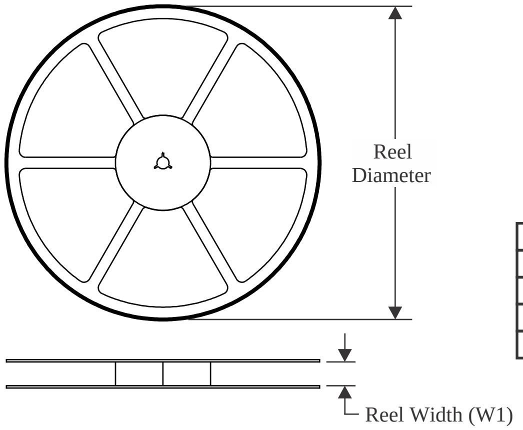
- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

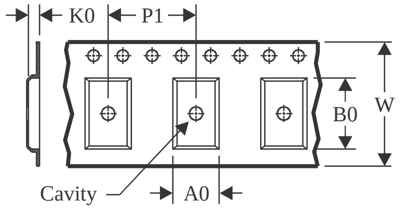
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

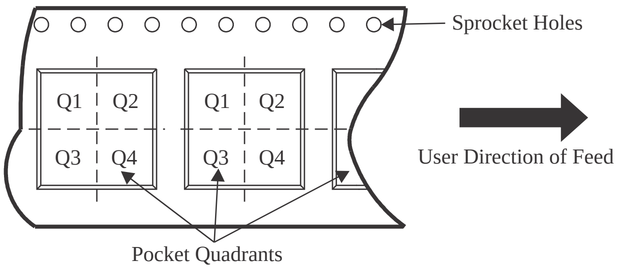


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



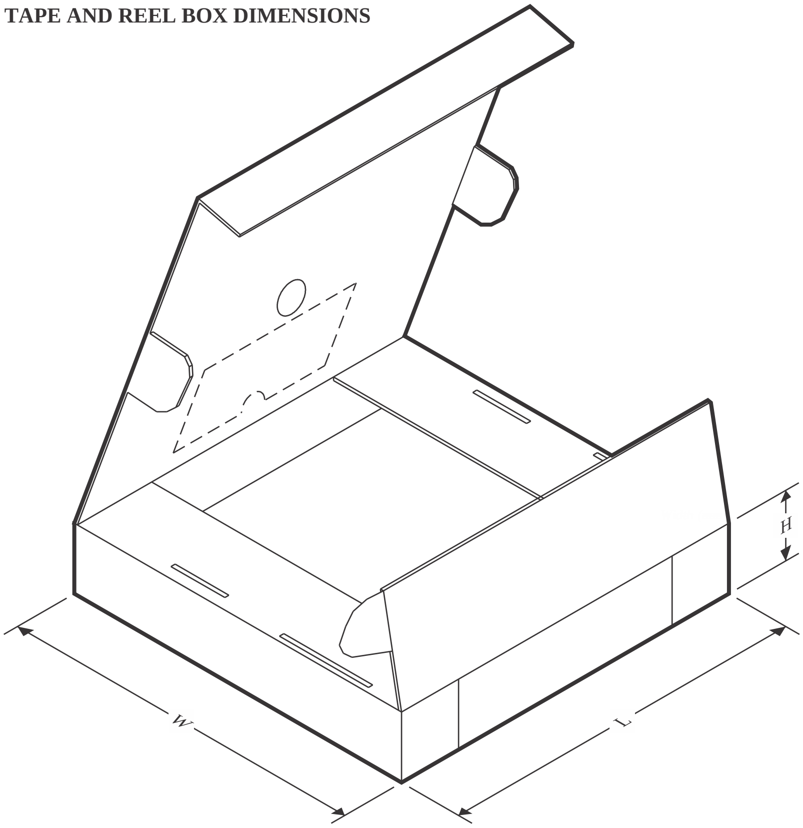
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL071ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL071HIDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL071HIDCKR	SC70	DCK	5	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3
TL071HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL071IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072ACDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072BCDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072CPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL072CPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

PACKAGE MATERIALS INFORMATION

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TL072HIDR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072HIPWR	TSSOP	PW	8	3000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL072IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TL074ACDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074ACNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074BCDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TL074CDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CDRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TL074CNSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	330.0	12.4	4.8	3.6	1.6	8.0	12.0	Q3
TL074HIPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL074IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

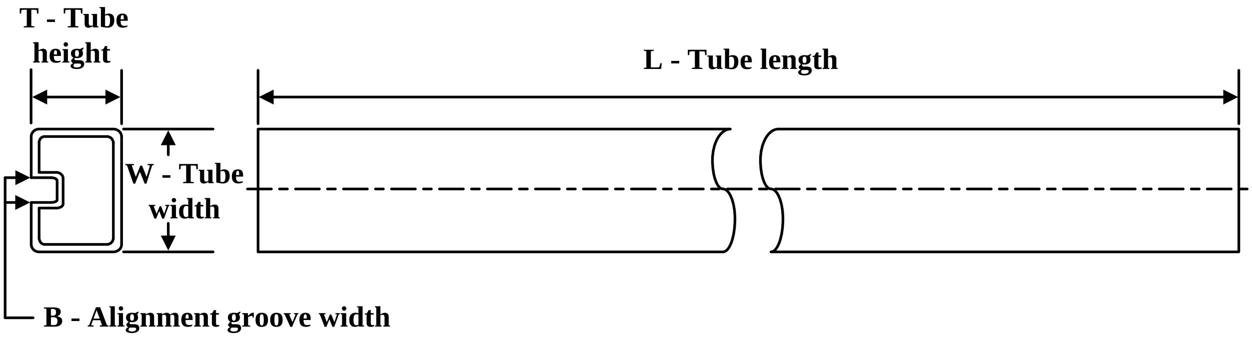


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL071ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL071CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL071CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL071HIDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TL071HIDCKR	SC70	DCK	5	3000	190.0	190.0	30.0
TL071HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL071IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072ACDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072BCDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072CDR	SOIC	D	8	2500	356.0	356.0	35.0
TL072CDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072CPSR	SO	PS	8	2000	356.0	356.0	35.0
TL072CPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TL072HIDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TL072HIDR	SOIC	D	8	3000	356.0	356.0	35.0
TL072HIPWR	TSSOP	PW	8	3000	356.0	356.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL072IDR	SOIC	D	8	2500	340.5	336.1	25.0
TL072IDR	SOIC	D	8	2500	356.0	356.0	35.0
TL074ACDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074ACNSR	SO	NS	14	2000	356.0	356.0	35.0
TL074BCDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074CDBR	SSOP	DB	14	2000	356.0	356.0	35.0
TL074CDR	SOIC	D	14	2500	340.5	336.1	32.0
TL074CDRG4	SOIC	D	14	2500	340.5	336.1	32.0
TL074CNSR	SO	NS	14	2000	356.0	356.0	35.0
TL074HIDYYR	SOT-23-THIN	DYY	14	3000	336.6	336.6	31.8
TL074HIPWR	TSSOP	PW	14	2000	356.0	356.0	35.0
TL074IDR	SOIC	D	14	2500	340.5	336.1	32.0

TUBE

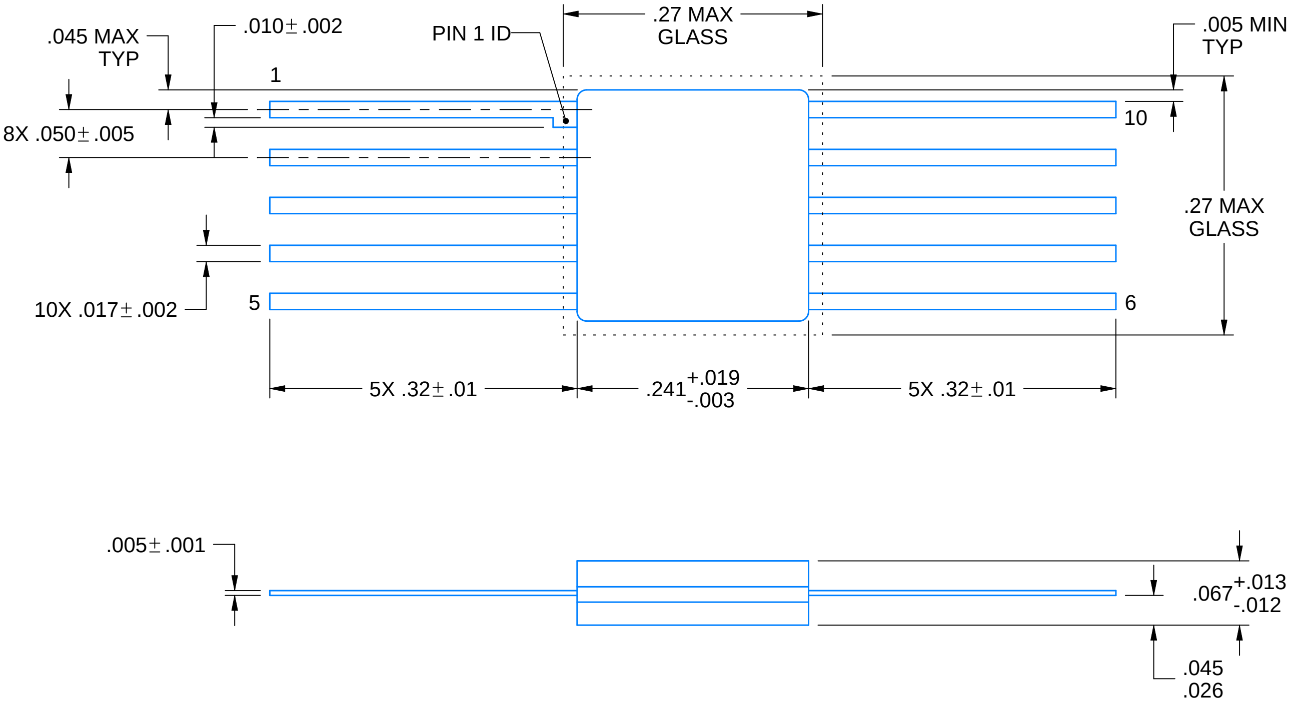


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
81023052A	FK	LCCC	20	1	506.98	12.06	2030	NA
8102305HA	U	CFP	10	1	506.98	26.16	6220	NA
81023062A	FK	LCCC	20	1	506.98	12.06	2030	NA
8102306DA	W	CFP	14	1	506.98	26.16	6220	NA
TL071ACD	D	SOIC	8	75	507	8	3940	4.32
TL071ACDG4	D	SOIC	8	75	507	8	3940	4.32
TL071ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL071BCD	D	SOIC	8	75	507	8	3940	4.32
TL071BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CD	D	SOIC	8	75	507	8	3940	4.32
TL071CD	D	SOIC	8	75	506.6	8	3940	4.32
TL071CP	P	PDIP	8	50	506	13.97	11230	4.32
TL071CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL071ID	D	SOIC	8	75	507	8	3940	4.32
TL071IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACD	D	SOIC	8	75	507	8	3940	4.32
TL072ACDE4	D	SOIC	8	75	507	8	3940	4.32
TL072ACP	P	PDIP	8	50	506	13.97	11230	4.32
TL072ACPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072BCD	D	SOIC	8	75	507	8	3940	4.32
TL072BCDE4	D	SOIC	8	75	507	8	3940	4.32
TL072BCDG4	D	SOIC	8	75	507	8	3940	4.32
TL072BCP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CD	D	SOIC	8	75	507	8	3940	4.32
TL072CD	D	SOIC	8	75	506.6	8	3940	4.32
TL072CDE4	D	SOIC	8	75	506.6	8	3940	4.32
TL072CDE4	D	SOIC	8	75	507	8	3940	4.32
TL072CDG4	D	SOIC	8	75	506.6	8	3940	4.32
TL072CDG4	D	SOIC	8	75	507	8	3940	4.32

PACKAGE MATERIALS INFORMATION

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TL072CP	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072CPS	PS	SOP	8	80	530	10.5	4000	4.1
TL072ID	D	SOIC	8	75	506.6	8	3940	4.32
TL072ID	D	SOIC	8	75	507	8	3940	4.32
TL072IDE4	D	SOIC	8	75	507	8	3940	4.32
TL072IDE4	D	SOIC	8	75	506.6	8	3940	4.32
TL072IDG4	D	SOIC	8	75	506.6	8	3940	4.32
TL072IDG4	D	SOIC	8	75	507	8	3940	4.32
TL072IP	P	PDIP	8	50	506	13.97	11230	4.32
TL072IPE4	P	PDIP	8	50	506	13.97	11230	4.32
TL072MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TL072MUB	U	CFP	10	1	506.98	26.16	6220	NA
TL074ACD	D	SOIC	14	50	507	8	3940	4.32
TL074ACDE4	D	SOIC	14	50	507	8	3940	4.32
TL074ACN	N	PDIP	14	25	506	13.97	11230	4.32
TL074ACNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCD	D	SOIC	14	50	507	8	3940	4.32
TL074BCDE4	D	SOIC	14	50	507	8	3940	4.32
TL074BCN	N	PDIP	14	25	506	13.97	11230	4.32
TL074BCNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CD	D	SOIC	14	50	507	8	3940	4.32
TL074CDG4	D	SOIC	14	50	507	8	3940	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CN	N	PDIP	14	25	506	13.97	11230	4.32
TL074CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CNE4	N	PDIP	14	25	506	13.97	11230	4.32
TL074CPW	PW	TSSOP	14	90	530	10.2	3600	3.5
TL074ID	D	SOIC	14	50	507	8	3940	4.32
TL074IDE4	D	SOIC	14	50	507	8	3940	4.32
TL074IDG4	D	SOIC	14	50	507	8	3940	4.32
TL074IN	N	PDIP	14	25	506	13.97	11230	4.32
TL074MFK	FK	LCCC	20	1	506.98	12.06	2030	NA
TL074MFKB	FK	LCCC	20	1	506.98	12.06	2030	NA
TL074MWB	W	CFP	14	1	506.98	26.16	6220	NA

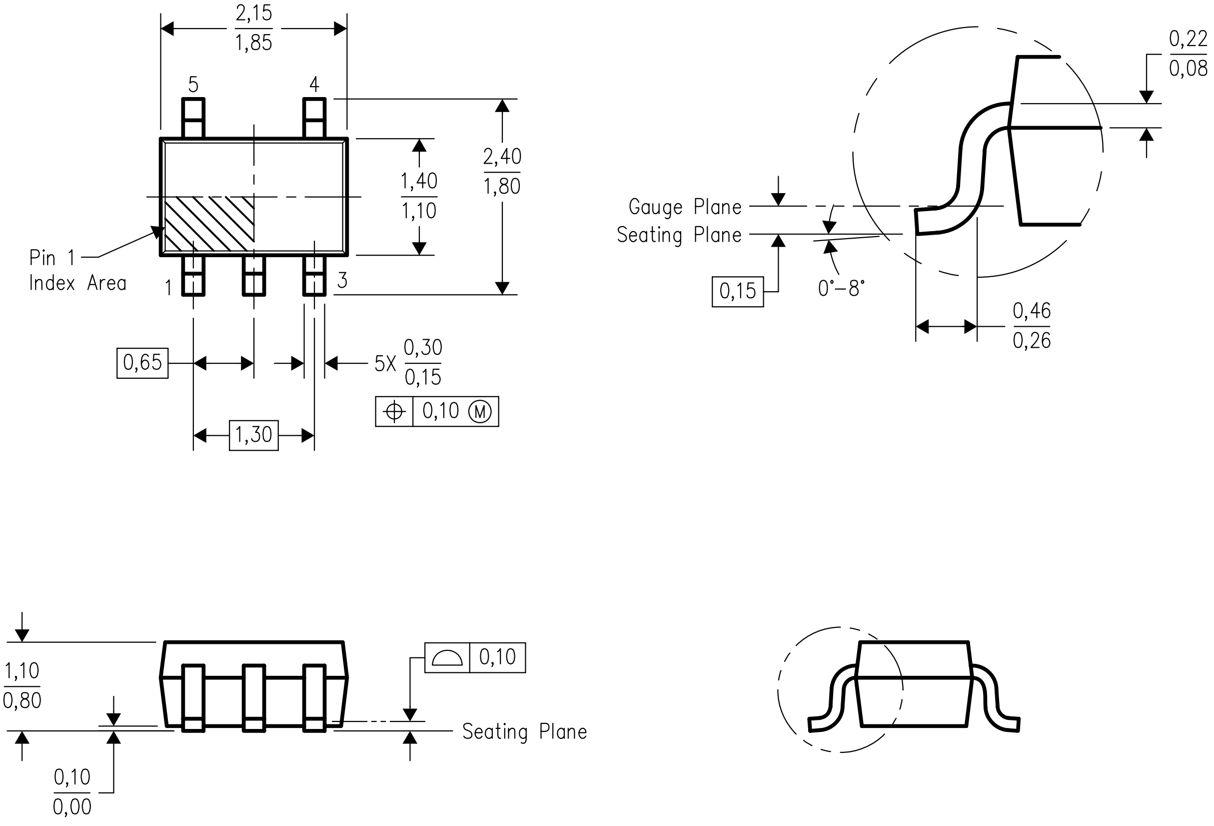


4225582/A 01/2020

NOTES:

1. All linear dimensions are in inches. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

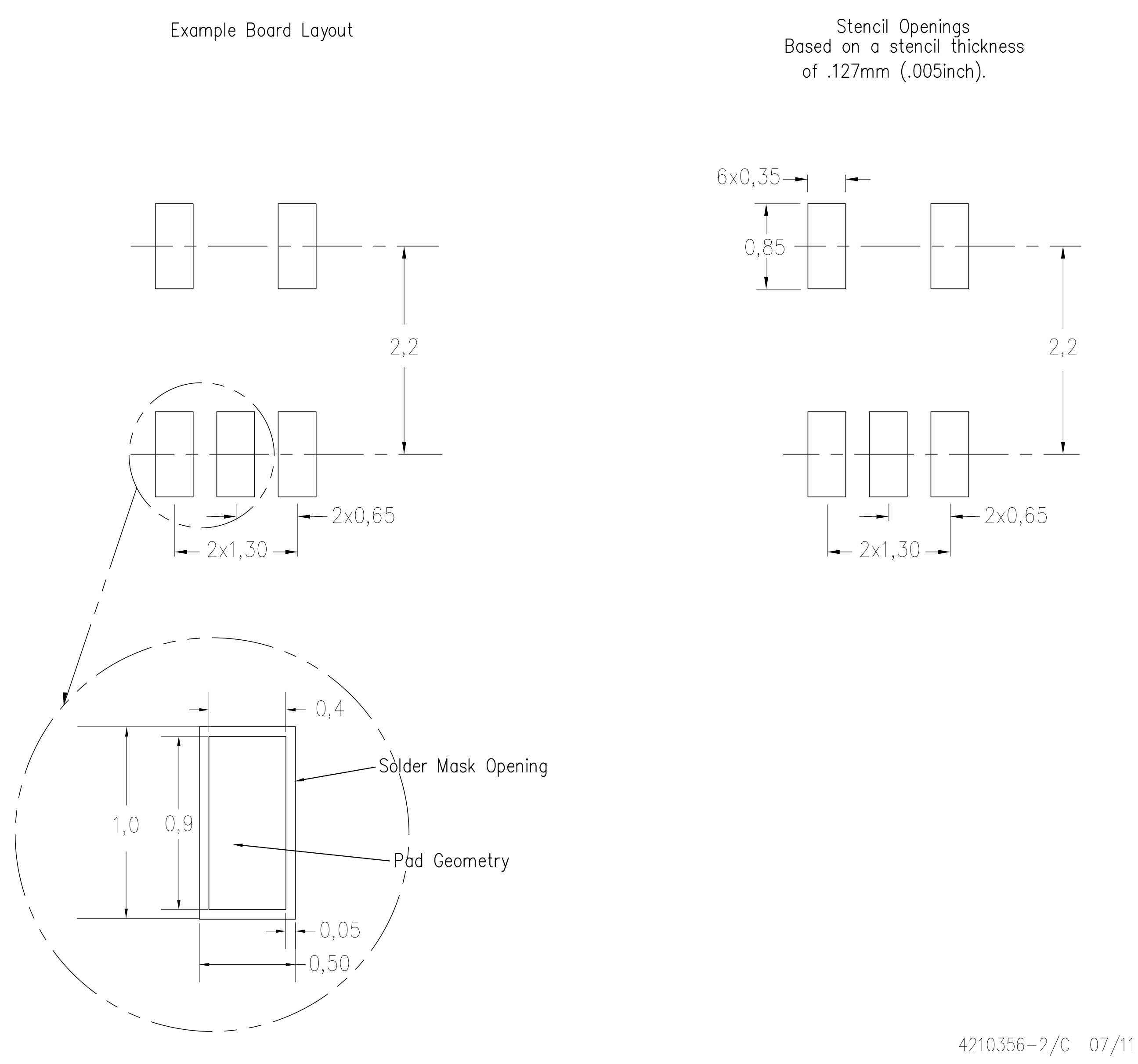
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553-3/G 01/2007

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

DCK (R–PDSO–G5) PLASTIC SMALL OUTLINE



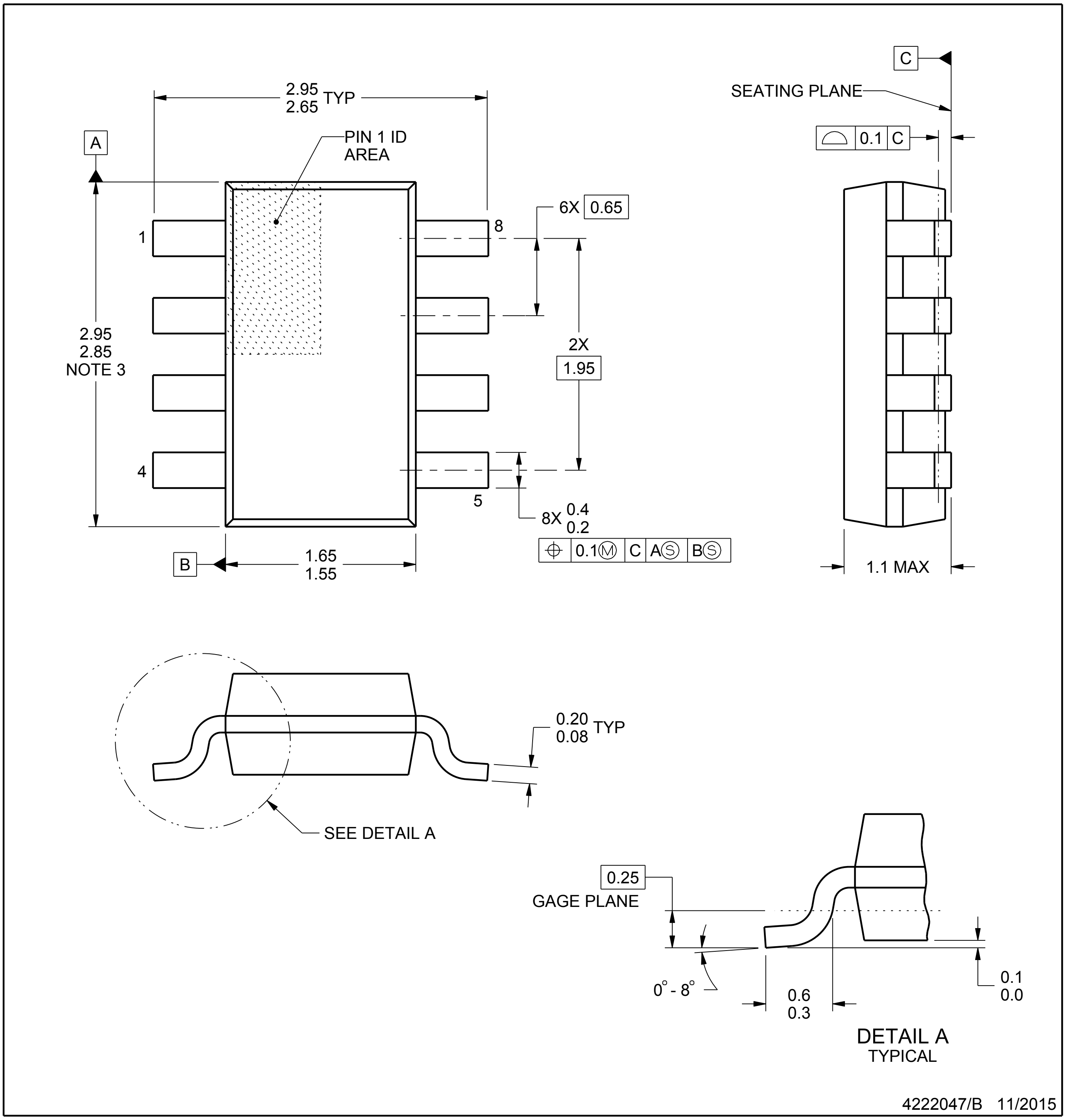
4210356-2/C 07/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. Publication IPC–7351 is recommended for alternate designs.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

DDF0008A

SOT-23 - 1.1 mm max height

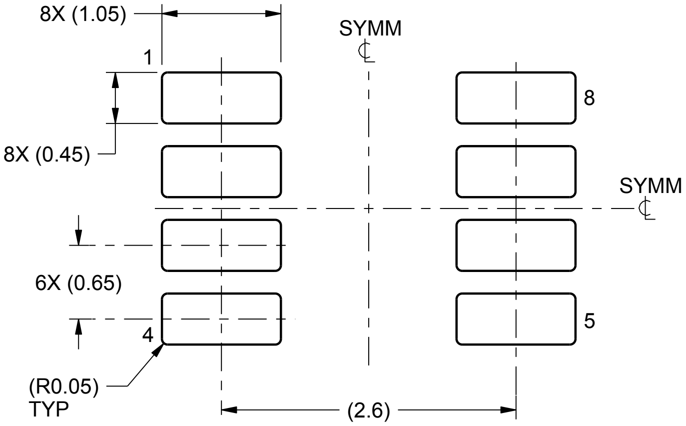
PLASTIC SMALL OUTLINE



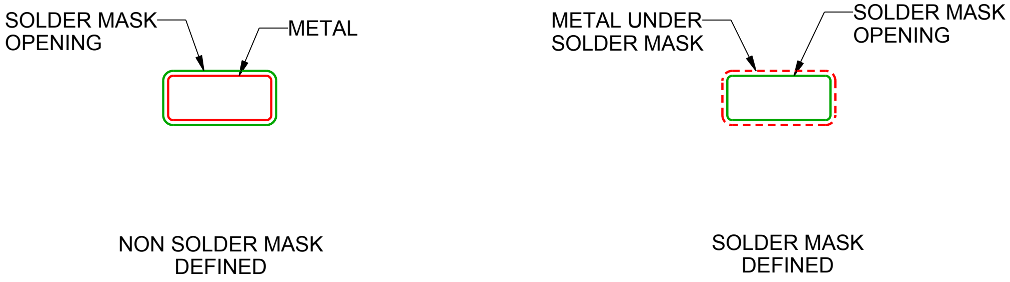
4222047/B 11/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



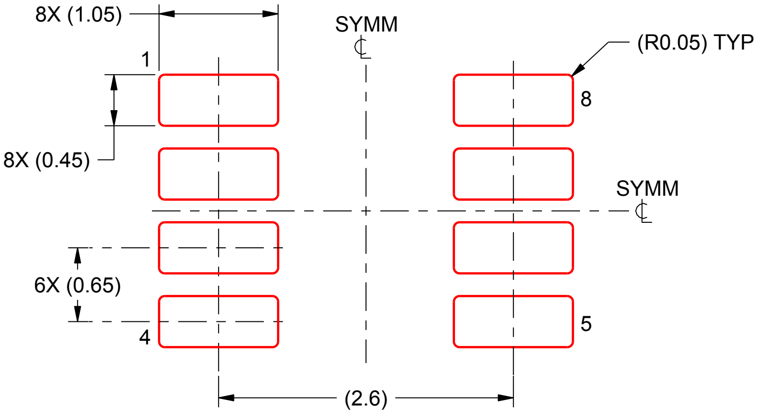
LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/B 11/2015

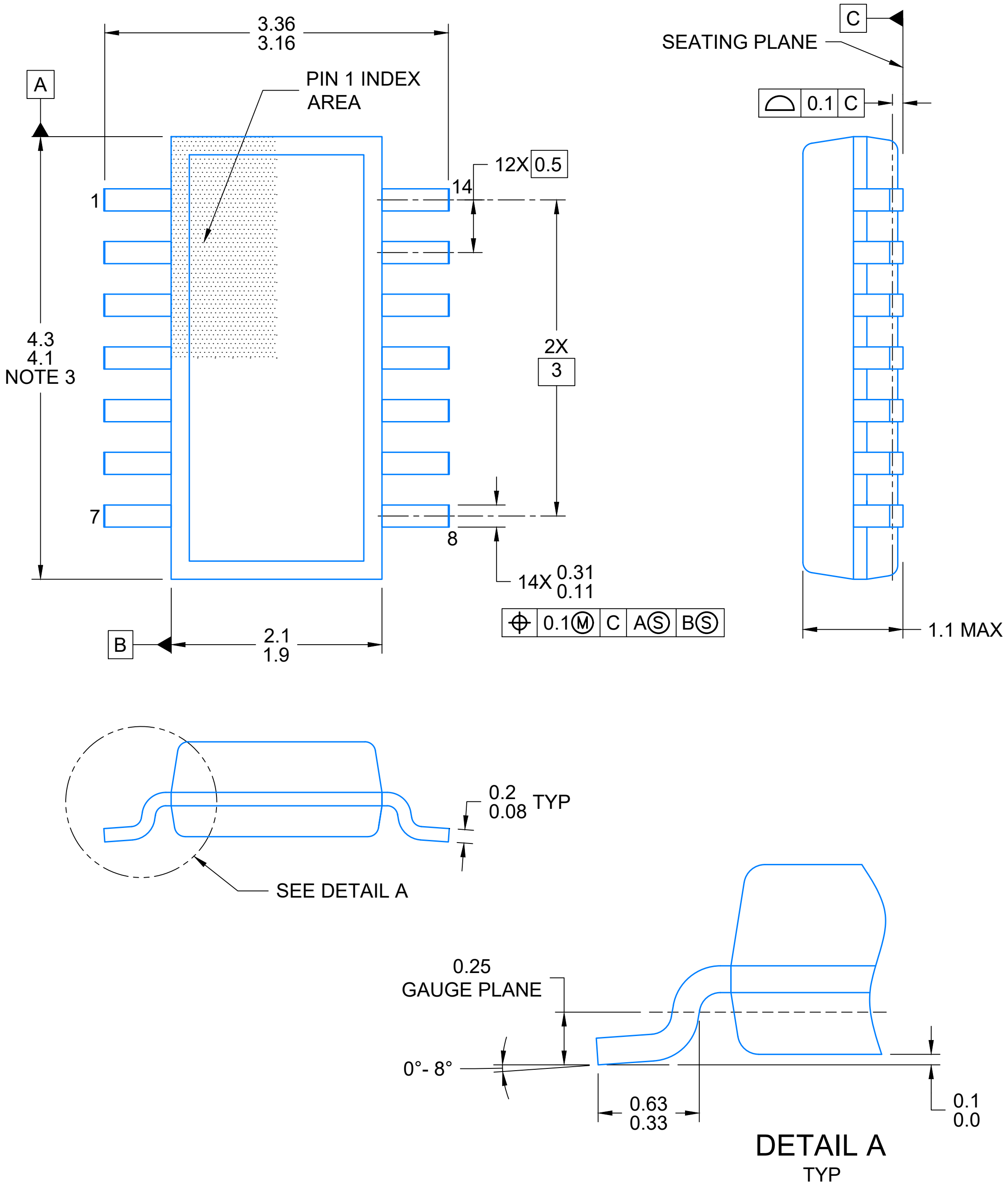
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

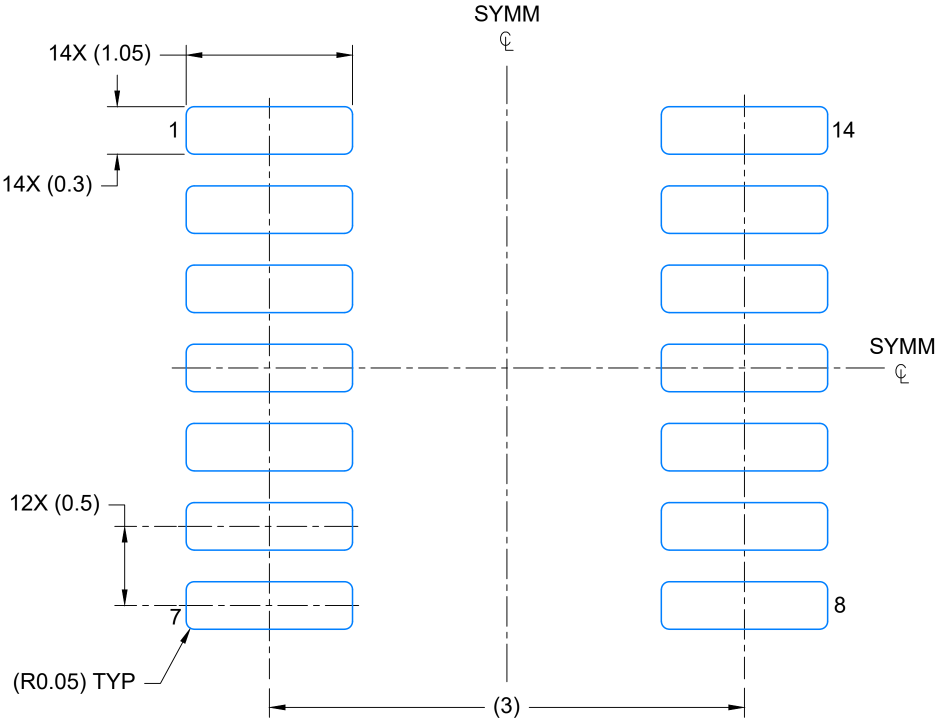
PLASTIC SMALL OUTLINE



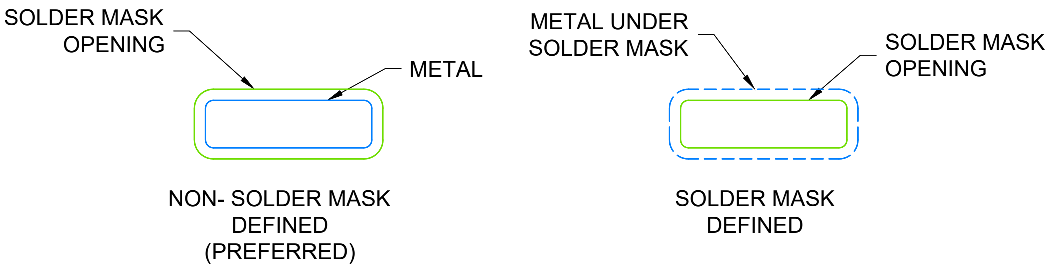
4224643/B 07/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB



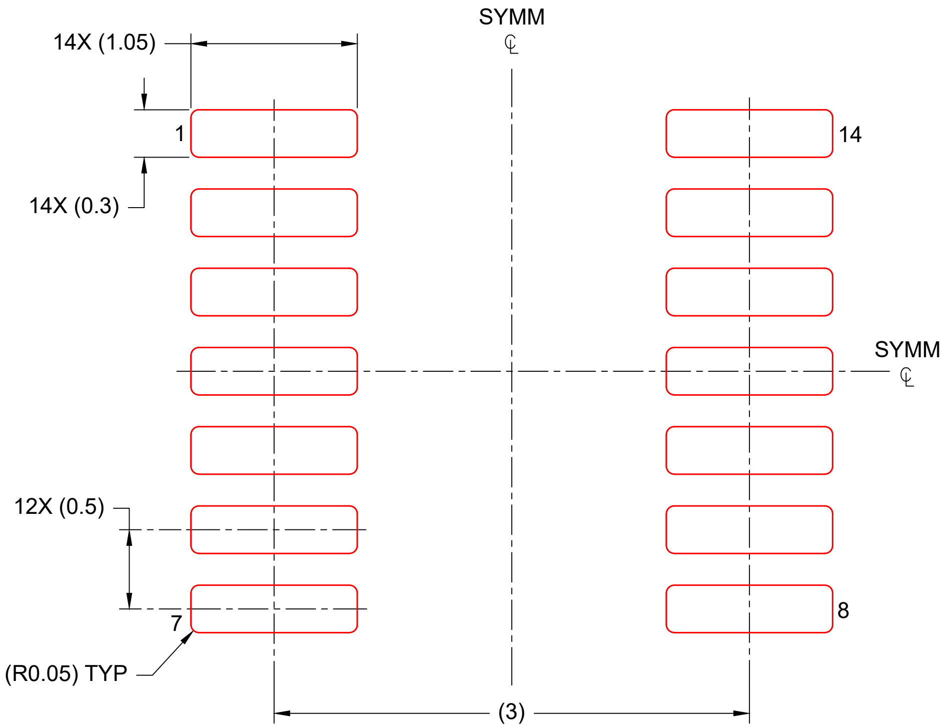
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/B 07/2021

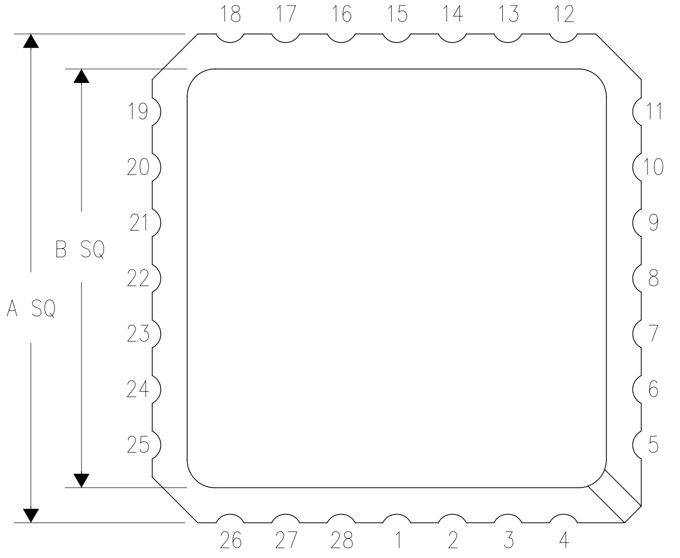
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

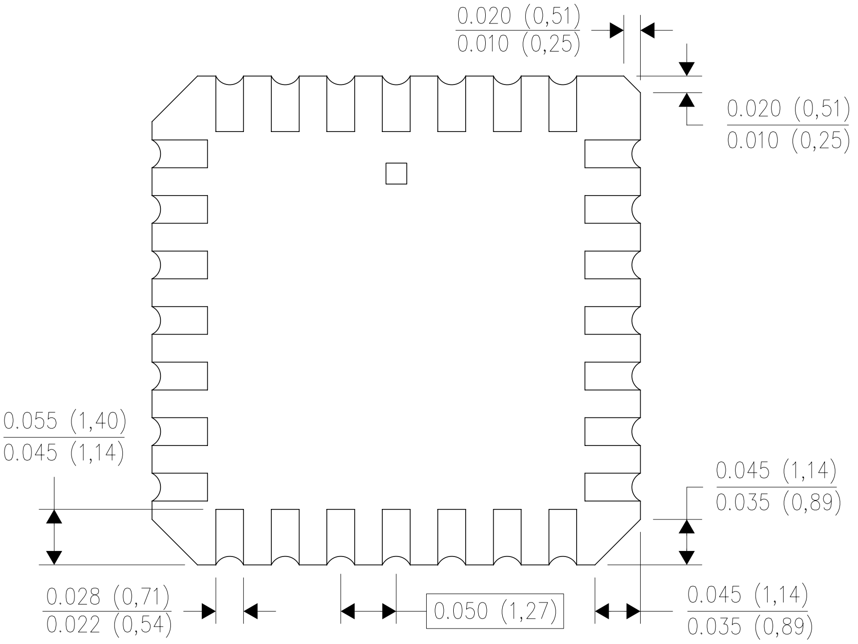
FK (S–CQCC–N**)

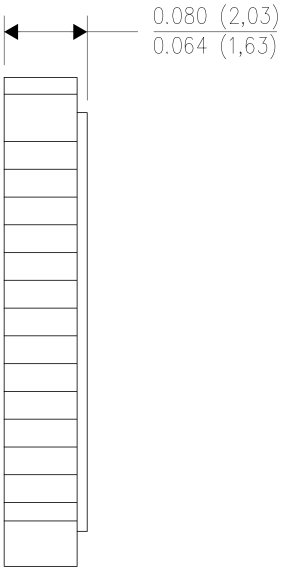
LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)





4040140/D 01/11

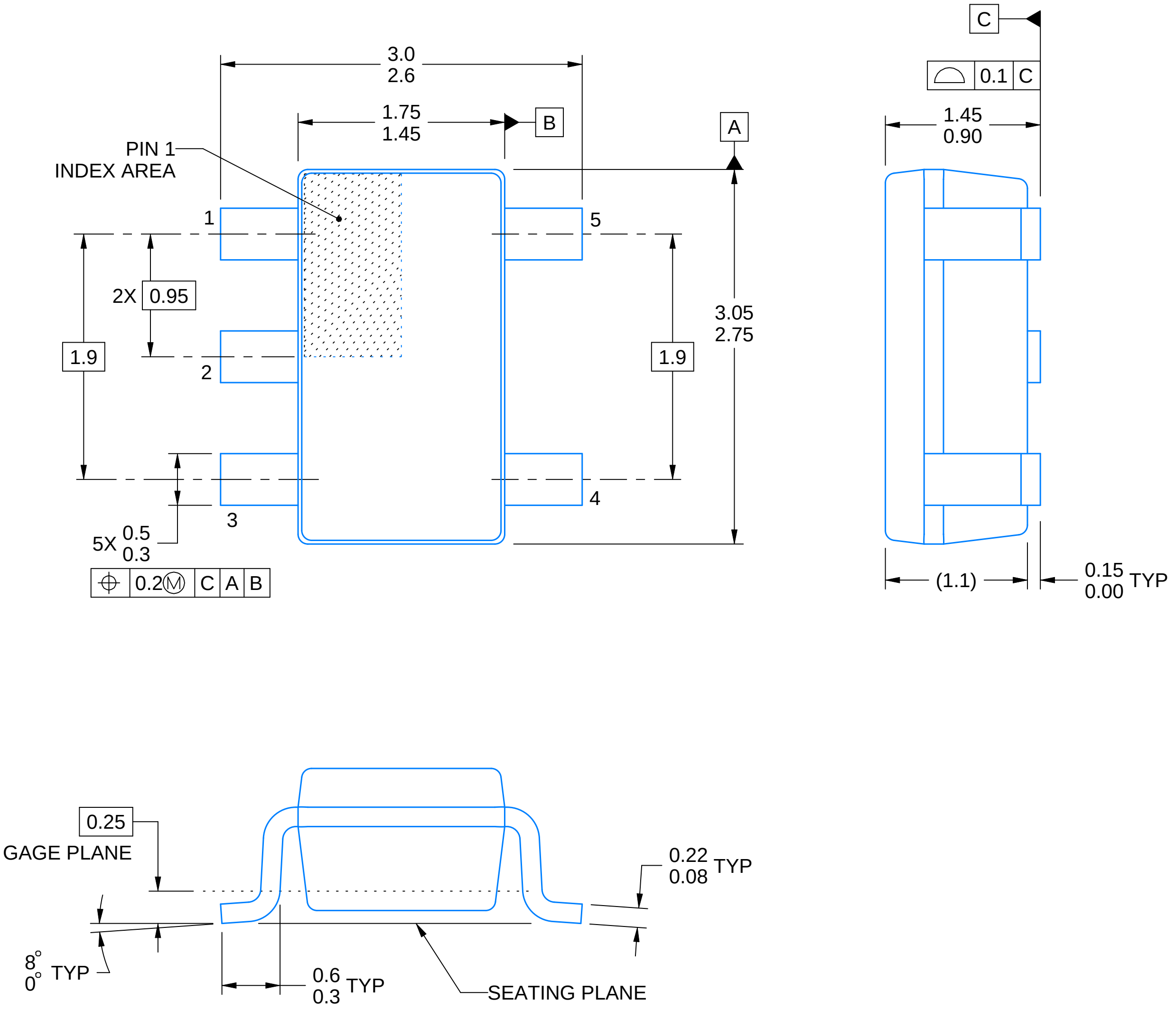
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS–004

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

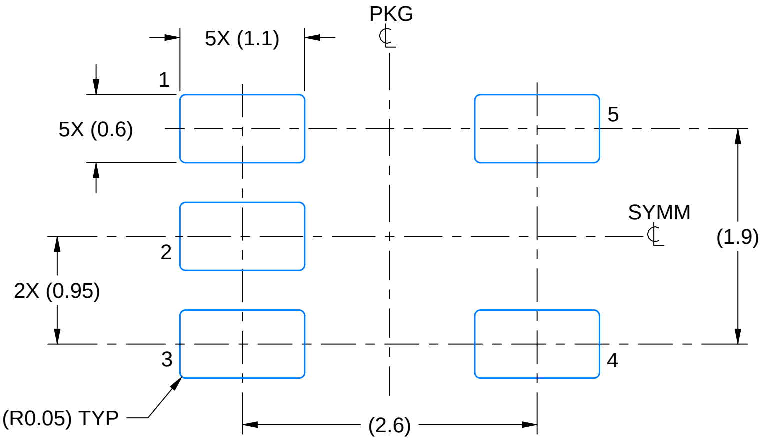
SMALL OUTLINE TRANSISTOR



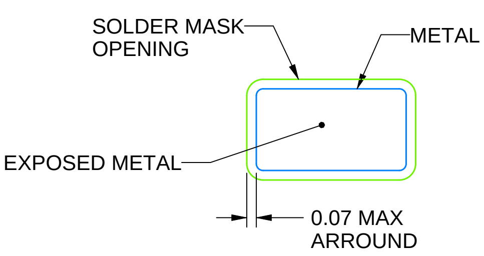
4214839/F 06/2021

NOTES:

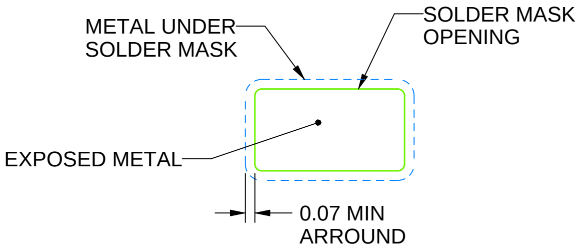
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK
DEFINED
(PREFERRED)

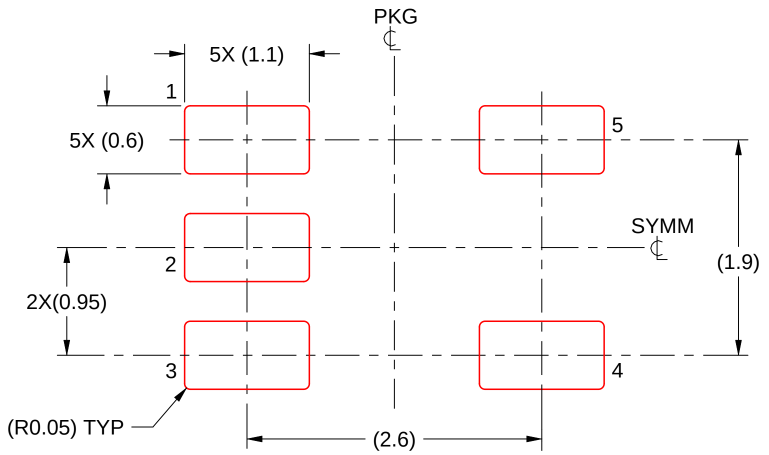


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

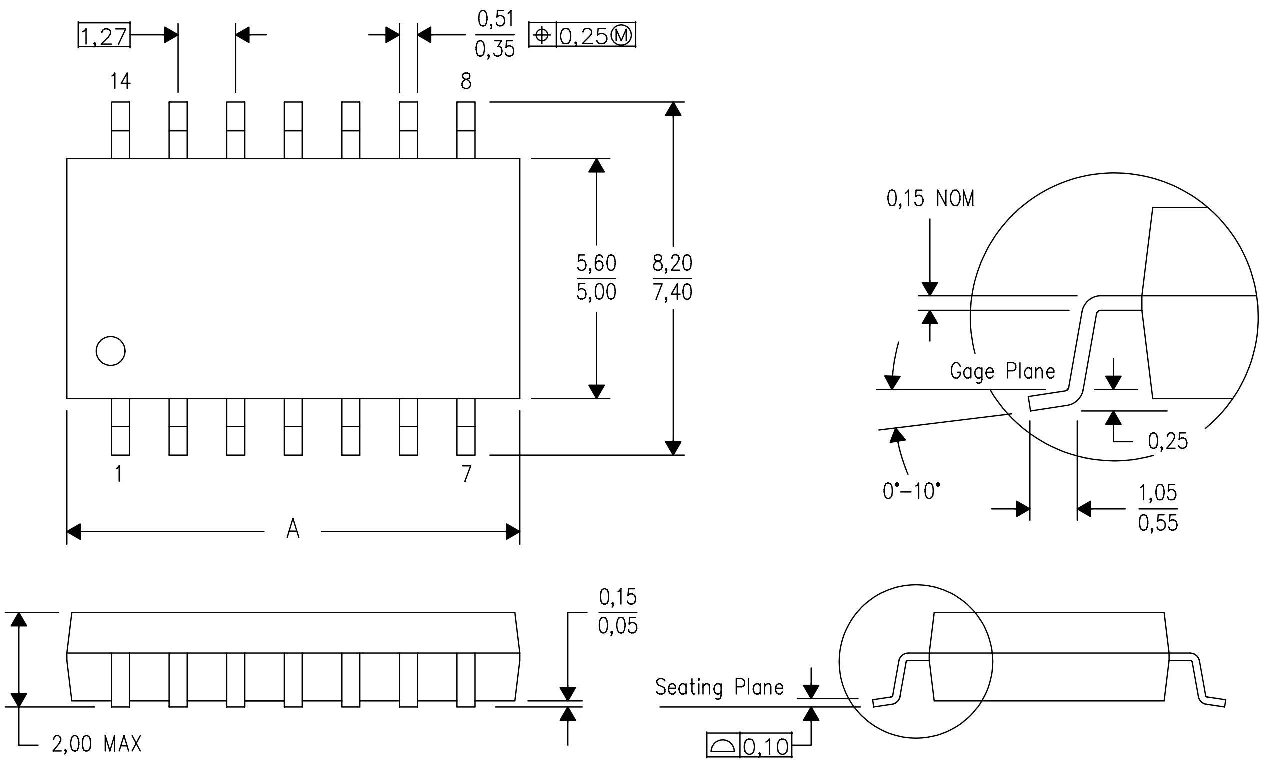
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

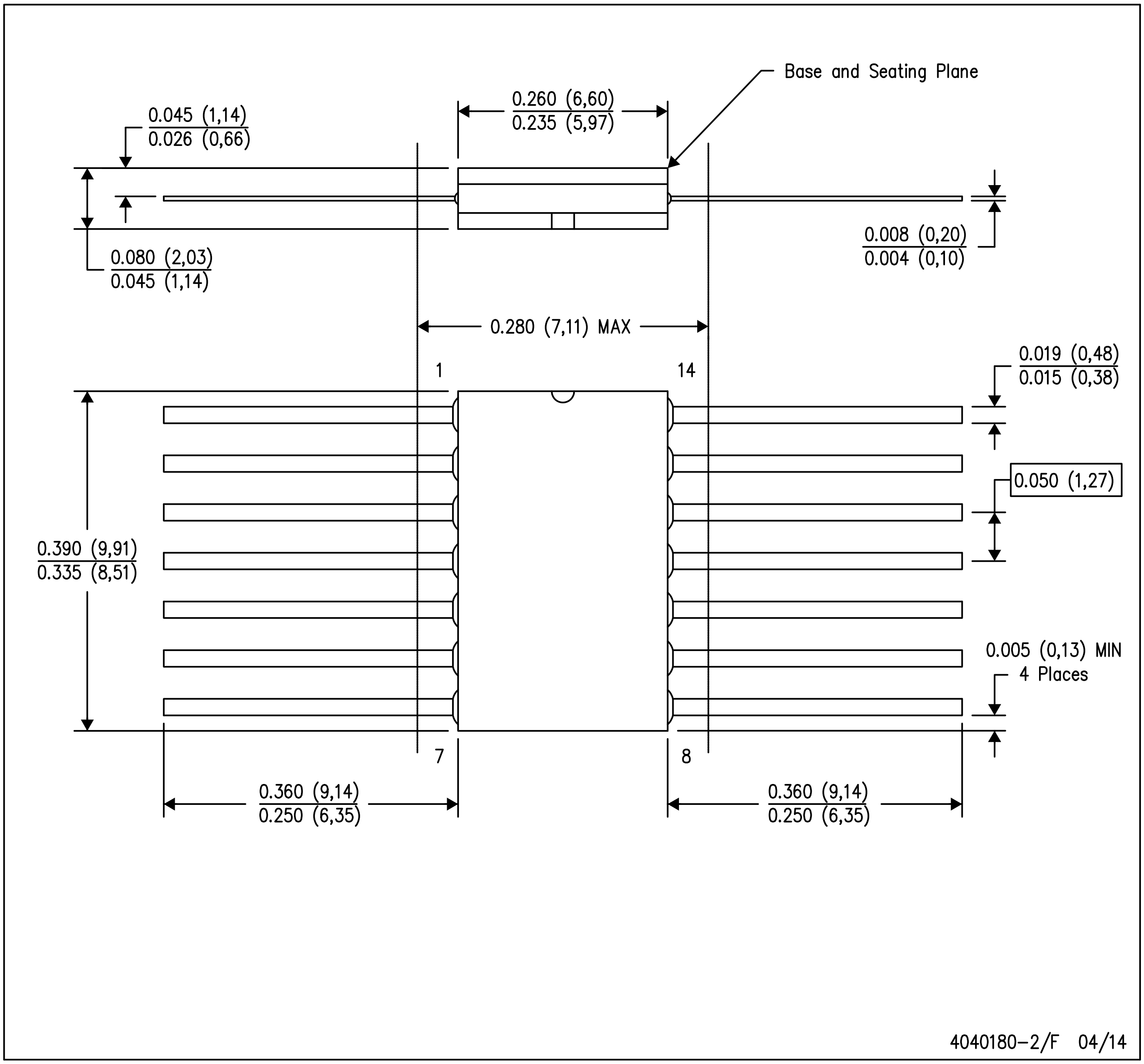


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

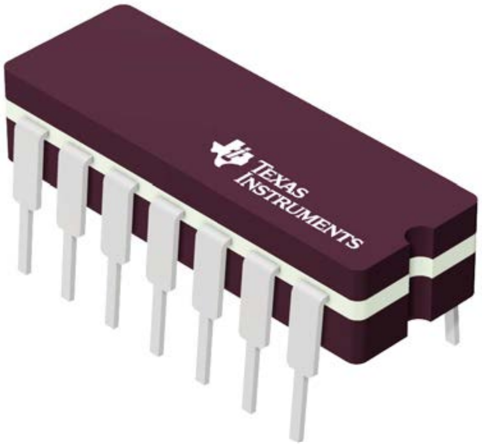
W (R–GDFP–F14) CERAMIC DUAL FLATPACK



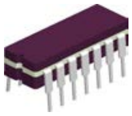
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

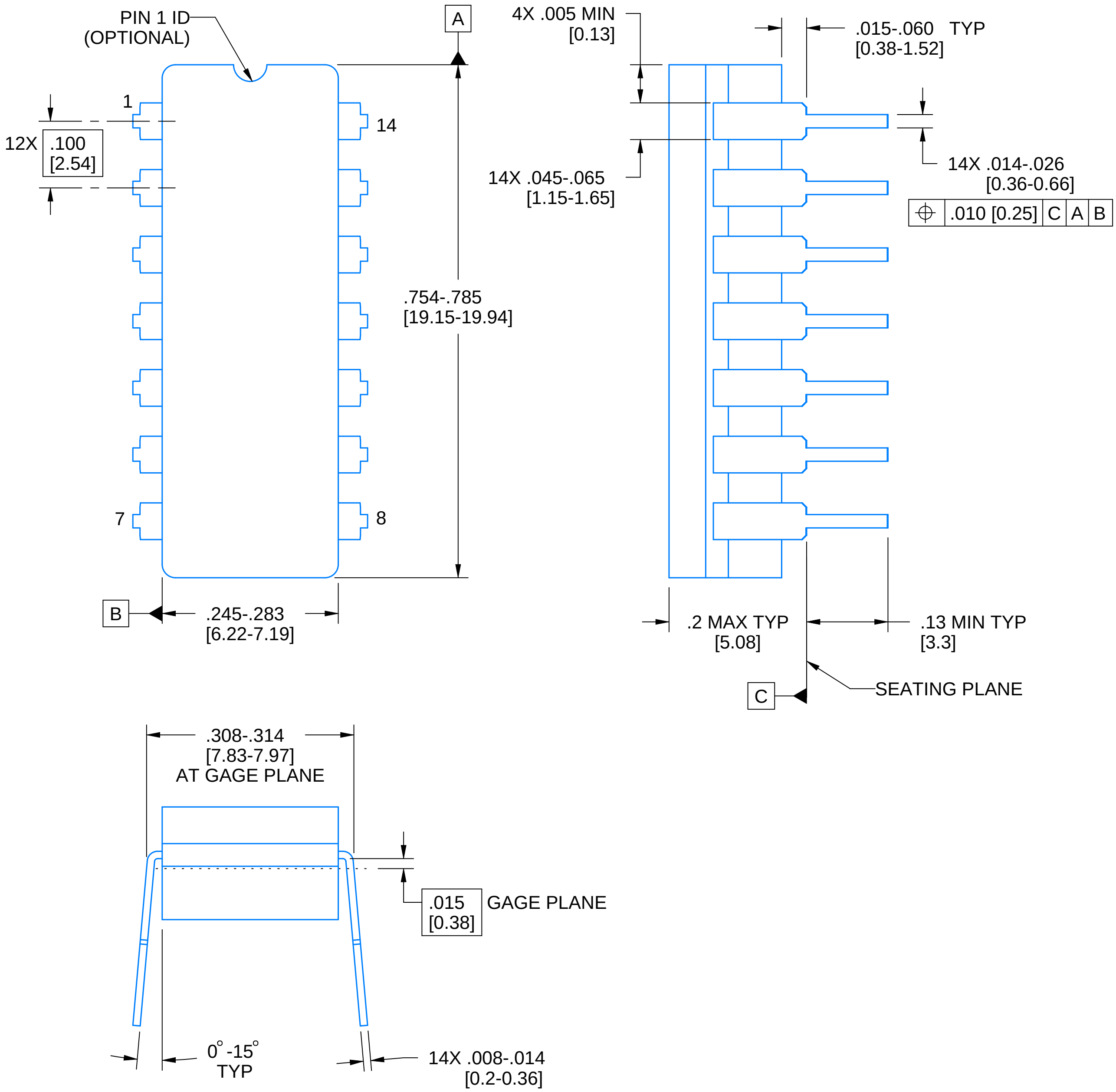


PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

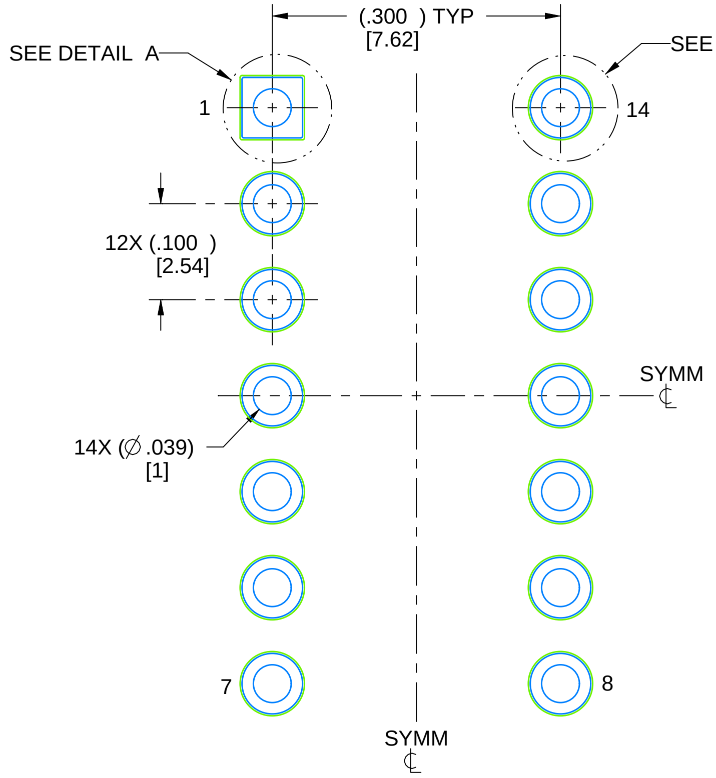
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

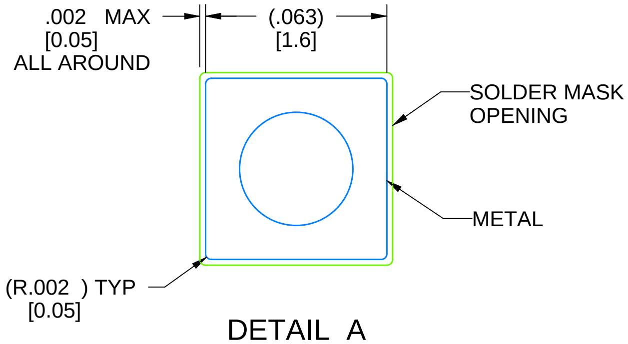
J0014A

CDIP - 5.08 mm max height

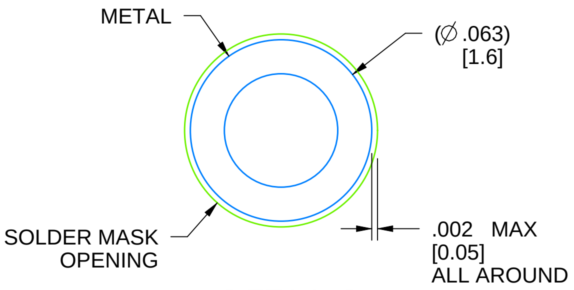
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



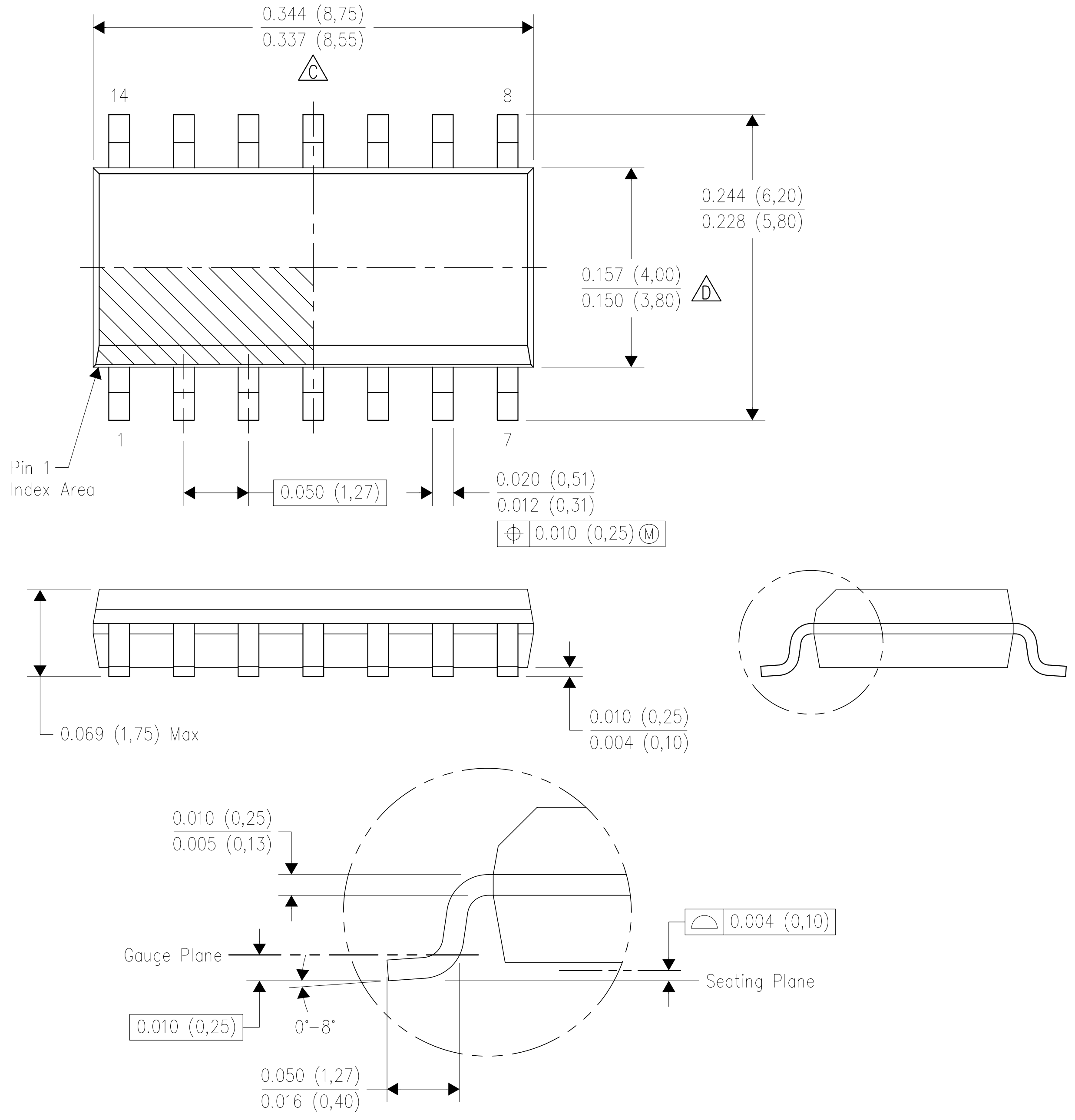
DETAIL A
SCALE: 15X



DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

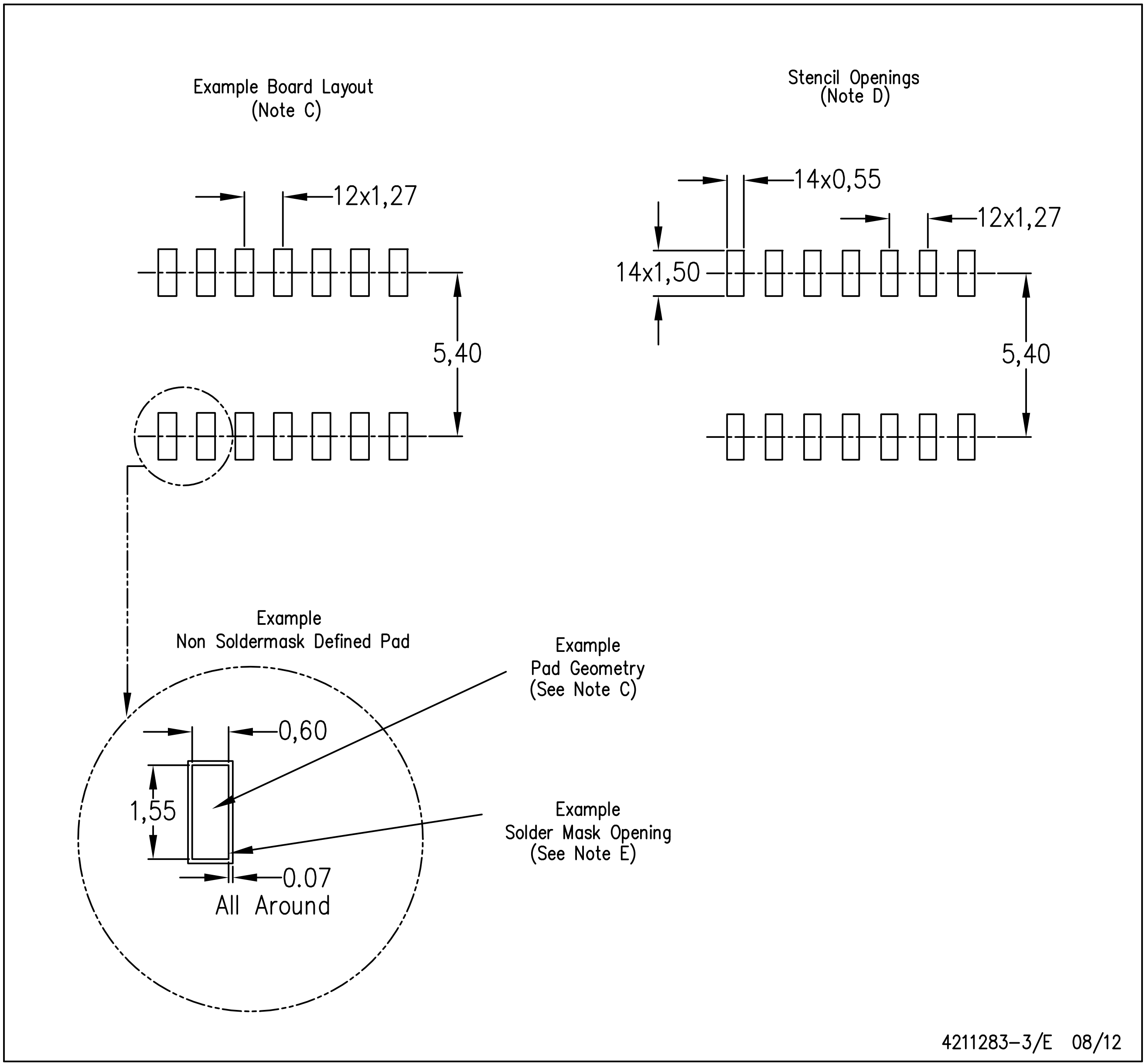
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- △C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- △D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS–012 variation AB.

D (R-PDSO-G14) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.

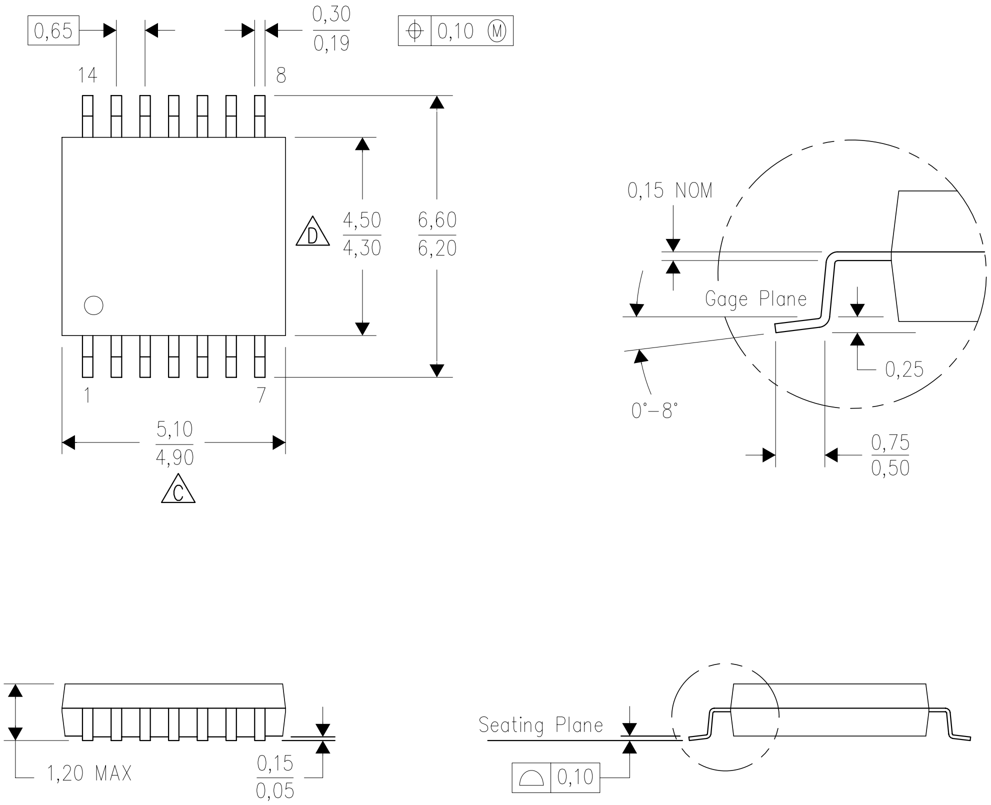
B. This drawing is subject to change without notice.

C. Publication IPC-7351 is recommended for alternate designs.

D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.

E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

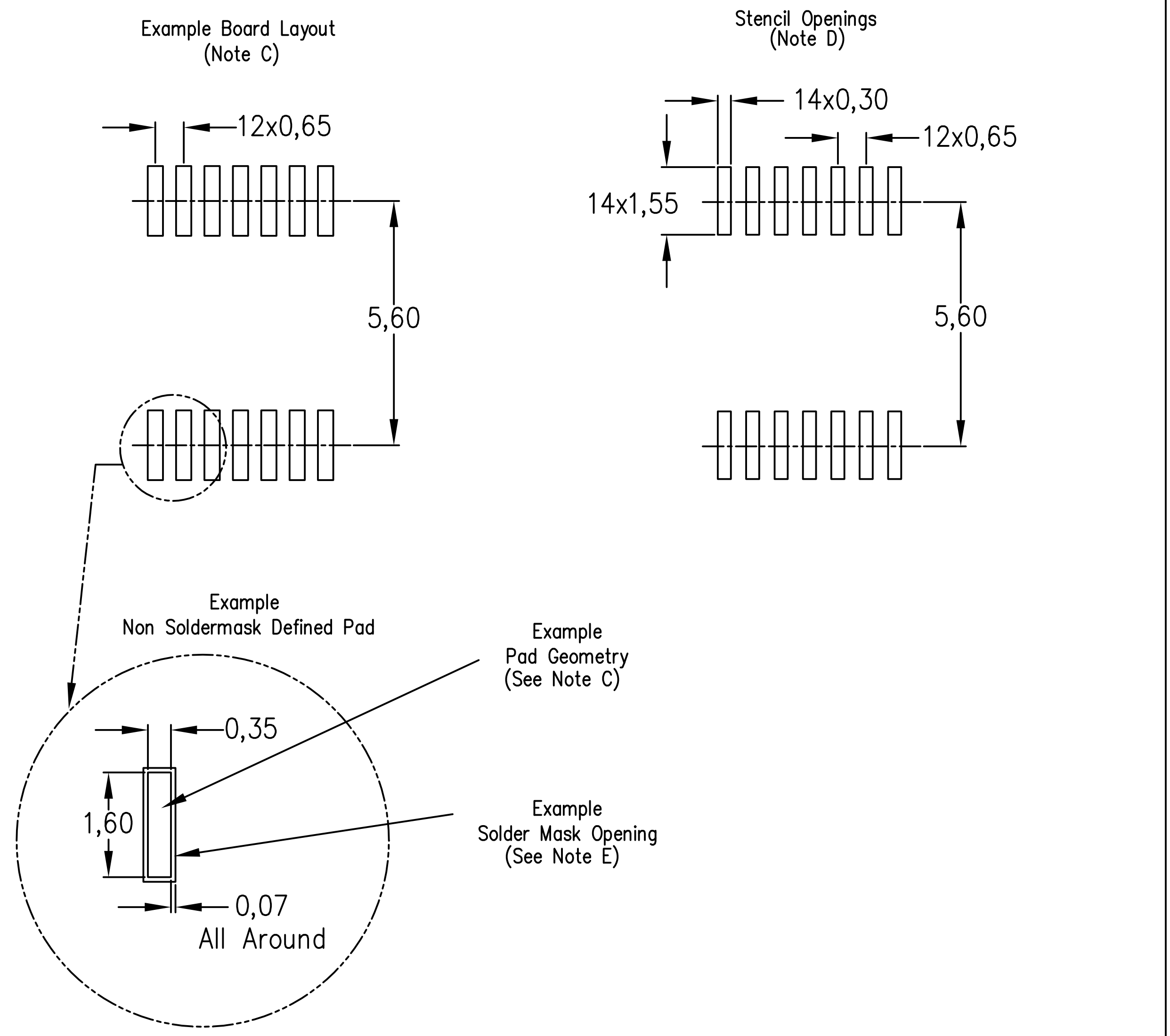
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

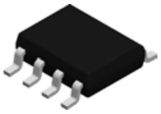
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4211284–2/G 08/15

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

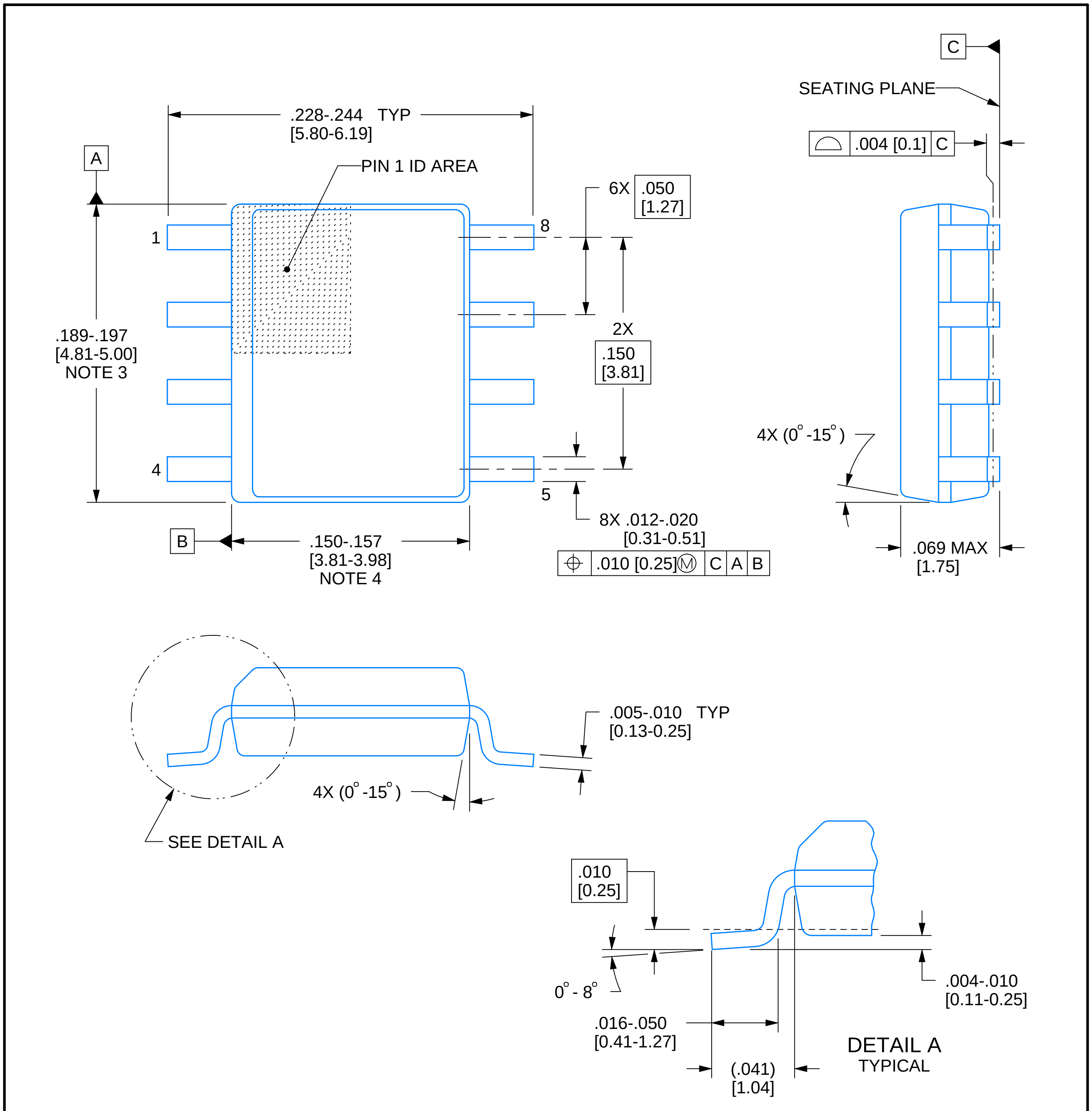


PACKAGE OUTLINE

D0008A

SOIC - 1.75 mm max height

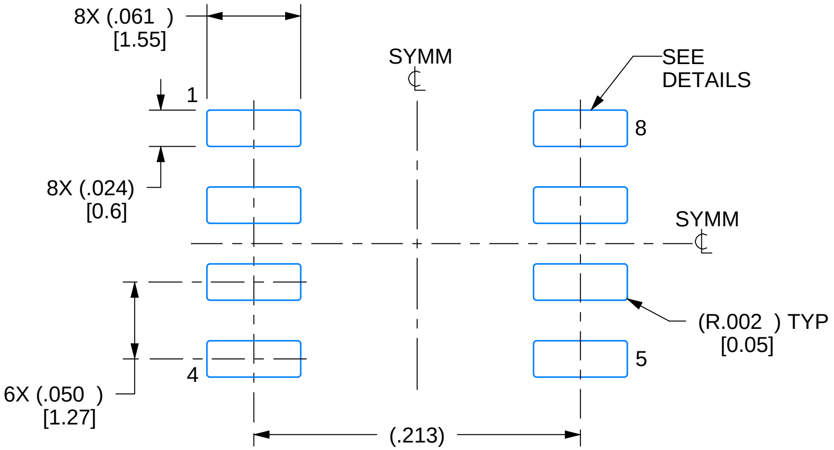
SMALL OUTLINE INTEGRATED CIRCUIT



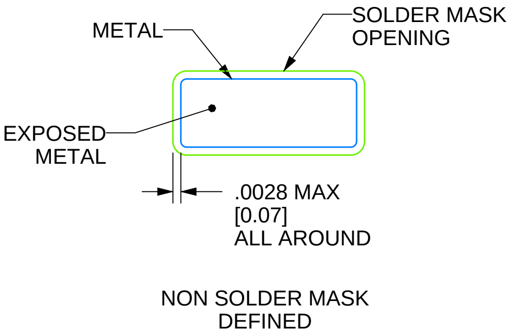
4214825/C 02/2019

NOTES:

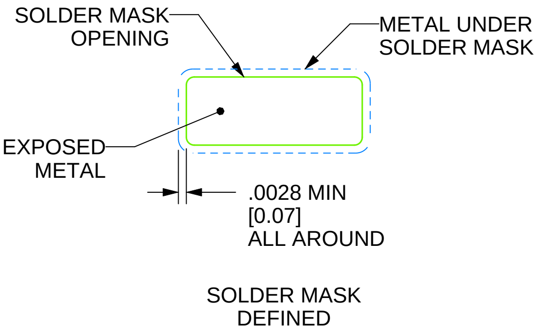
1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



NON SOLDER MASK
DEFINED

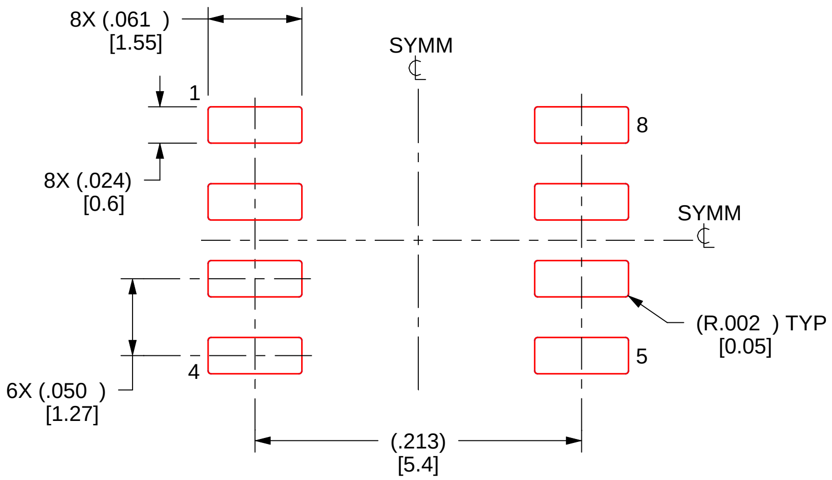


SOLDER MASK
DEFINED

SOLDER MASK DETAILS

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



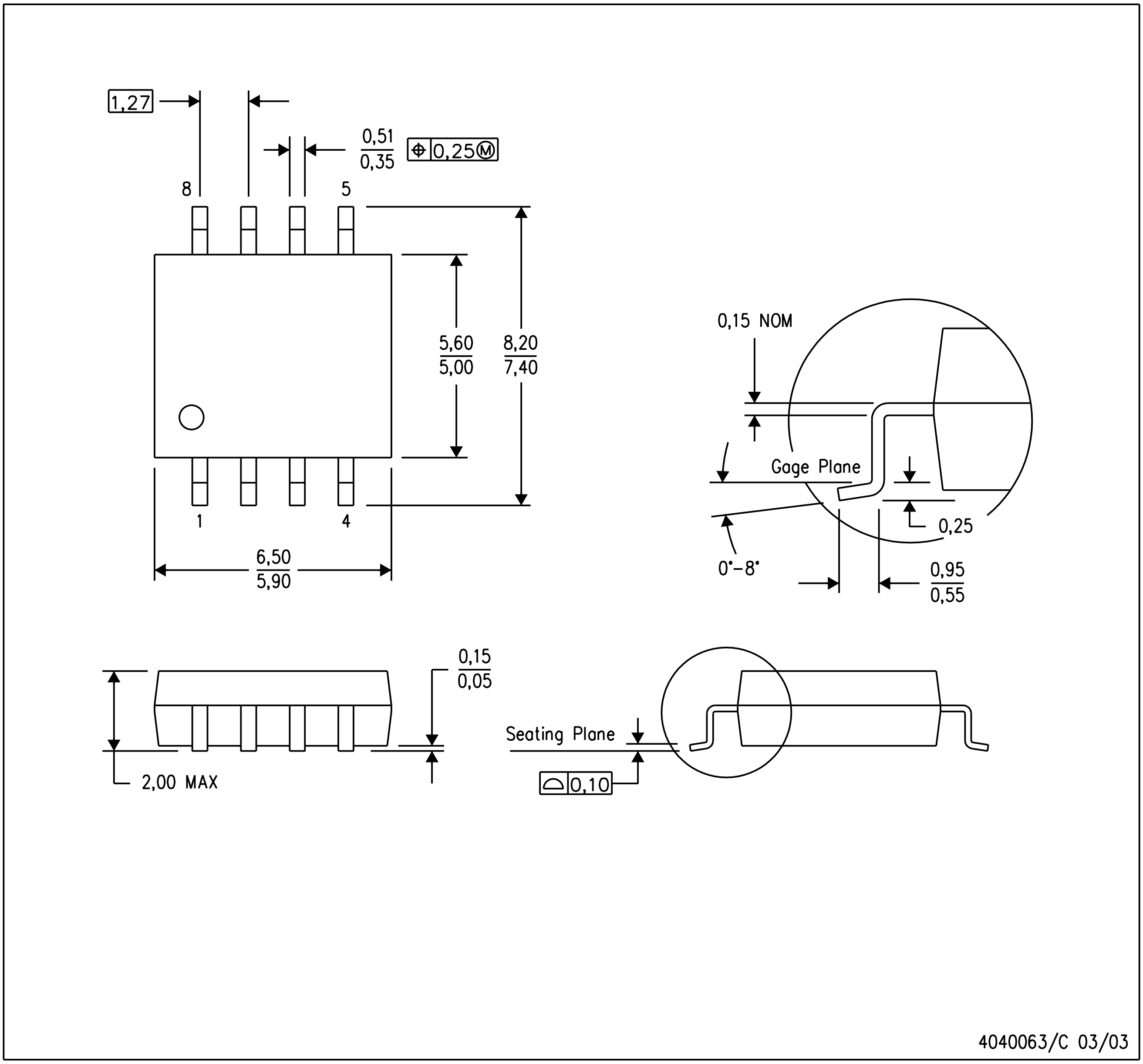
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

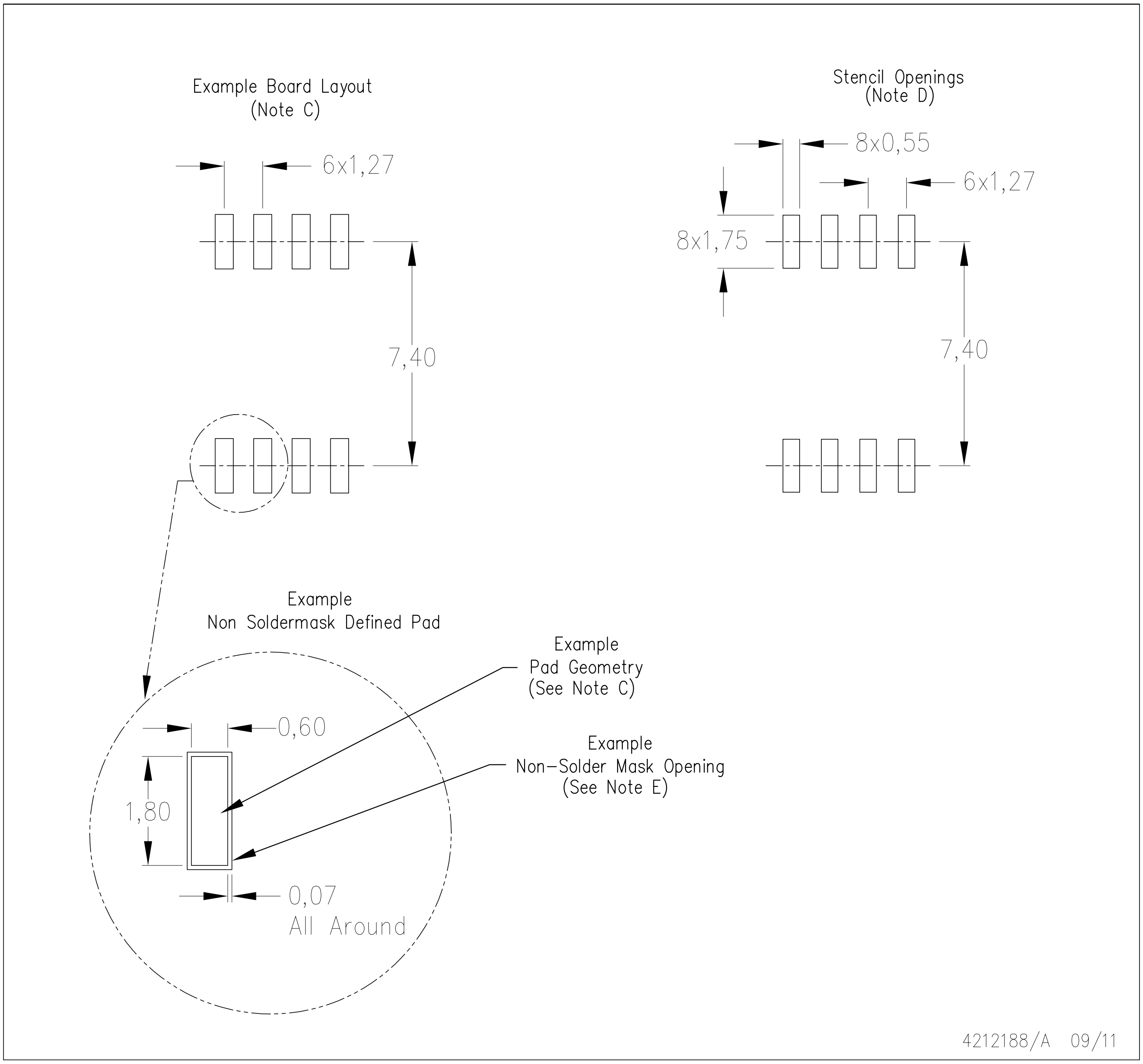
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



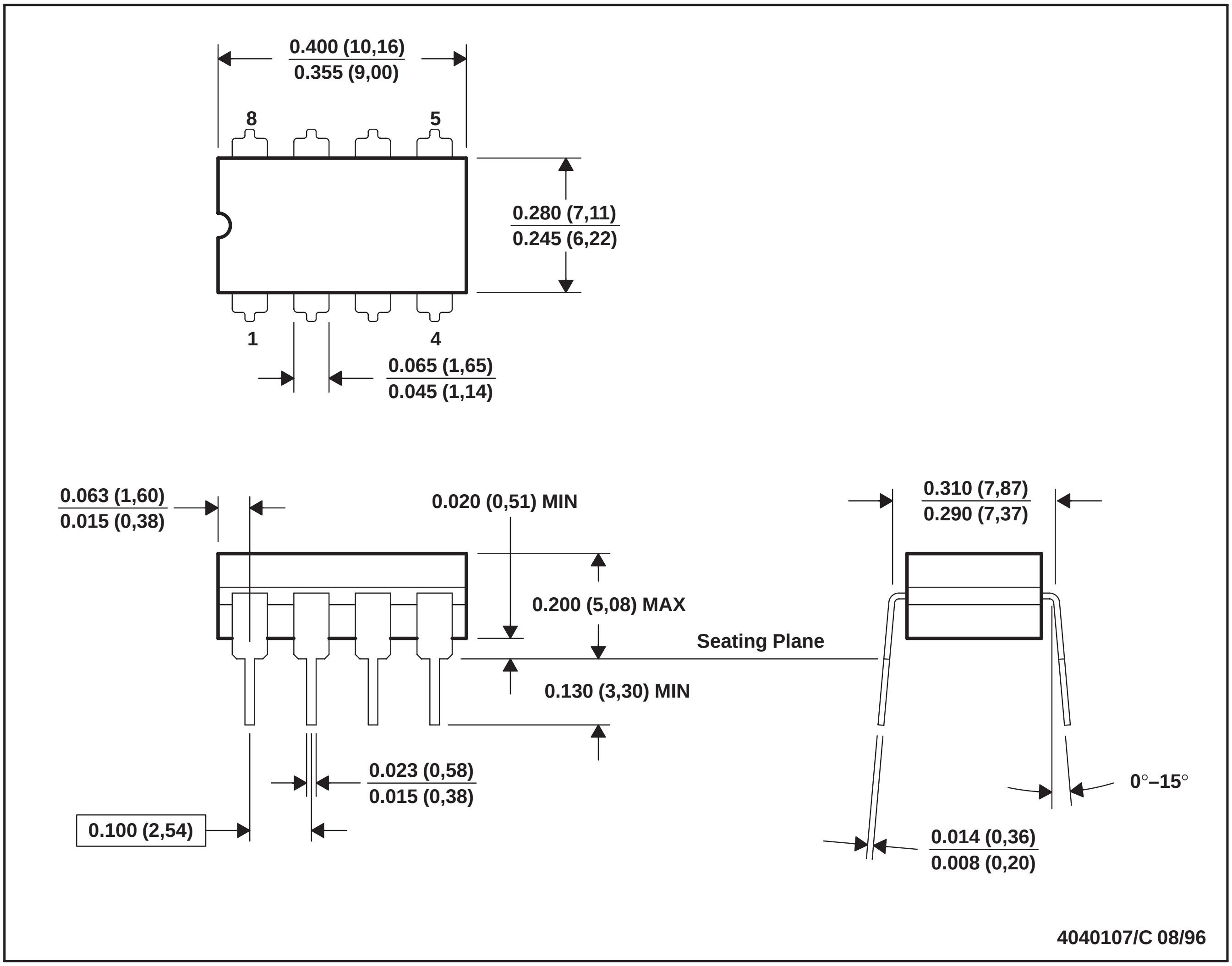
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PS (R-PDSO-G8) PLASTIC SMALL OUTLINE



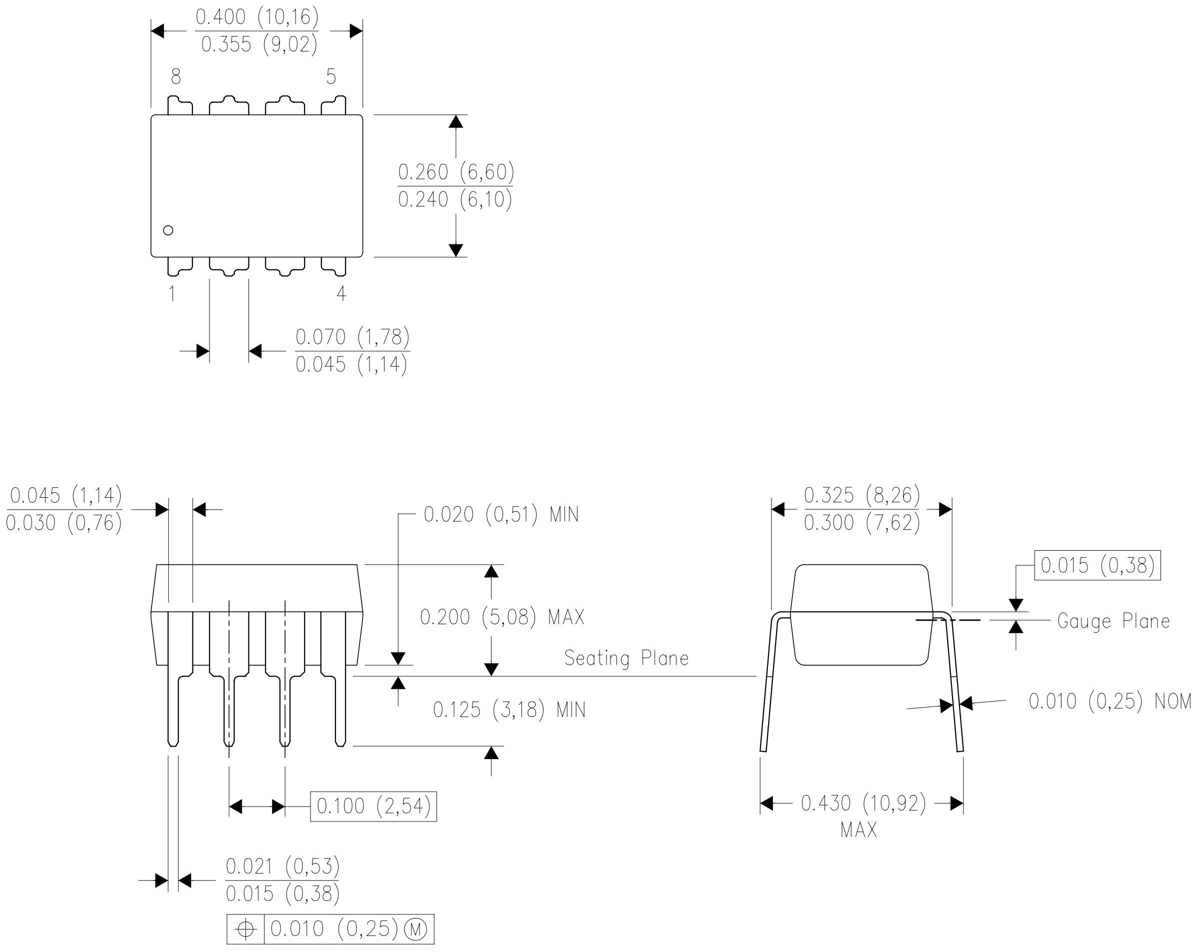
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

JG (R-GDIP-T8) **CERAMIC DUAL-IN-LINE**



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification.
- E. Falls within MIL STD 1835 GDIP1-T8

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE

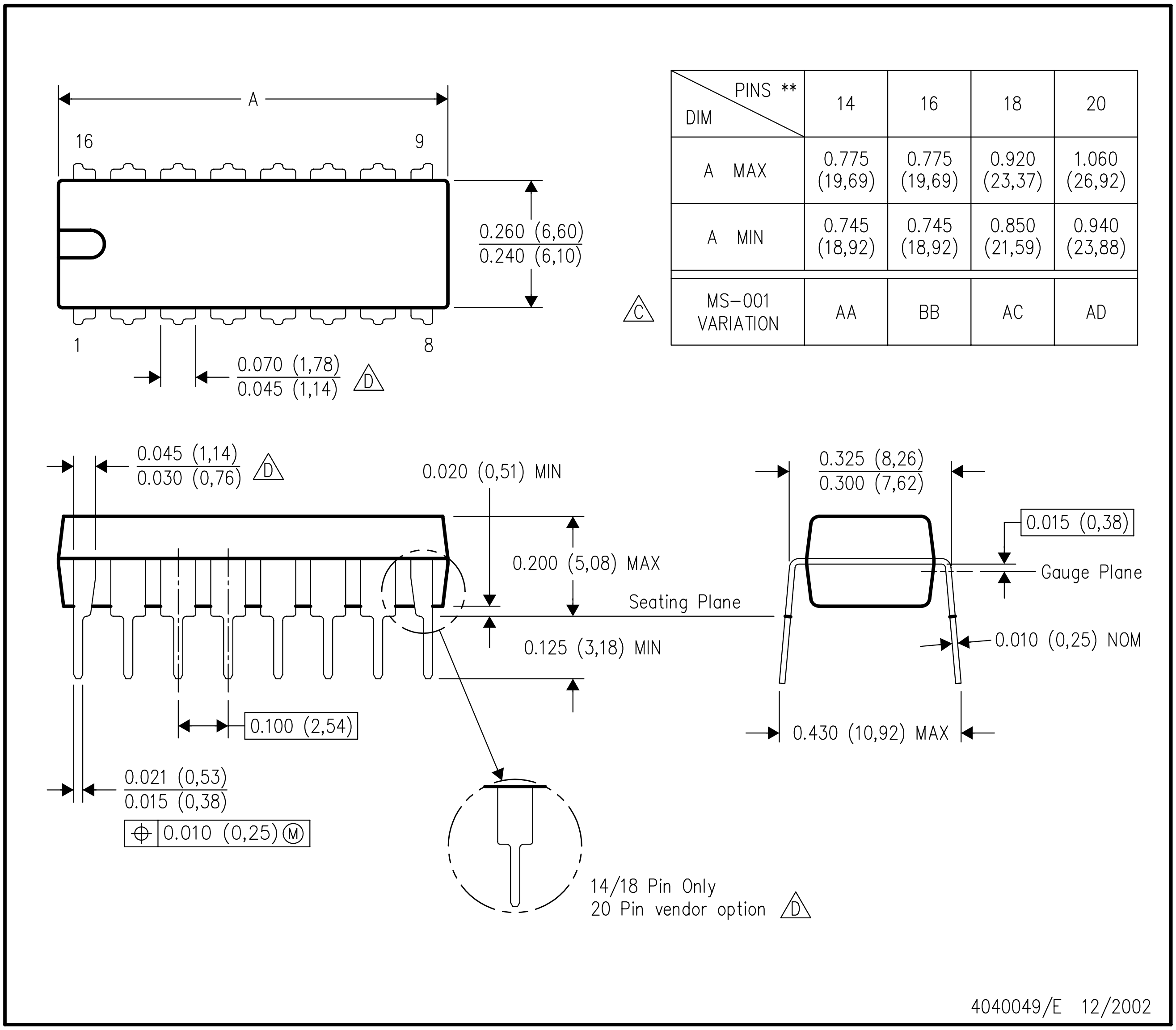


4040082/E 04/2010

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001 variation BA.

N (R–PDIP–T**)   PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

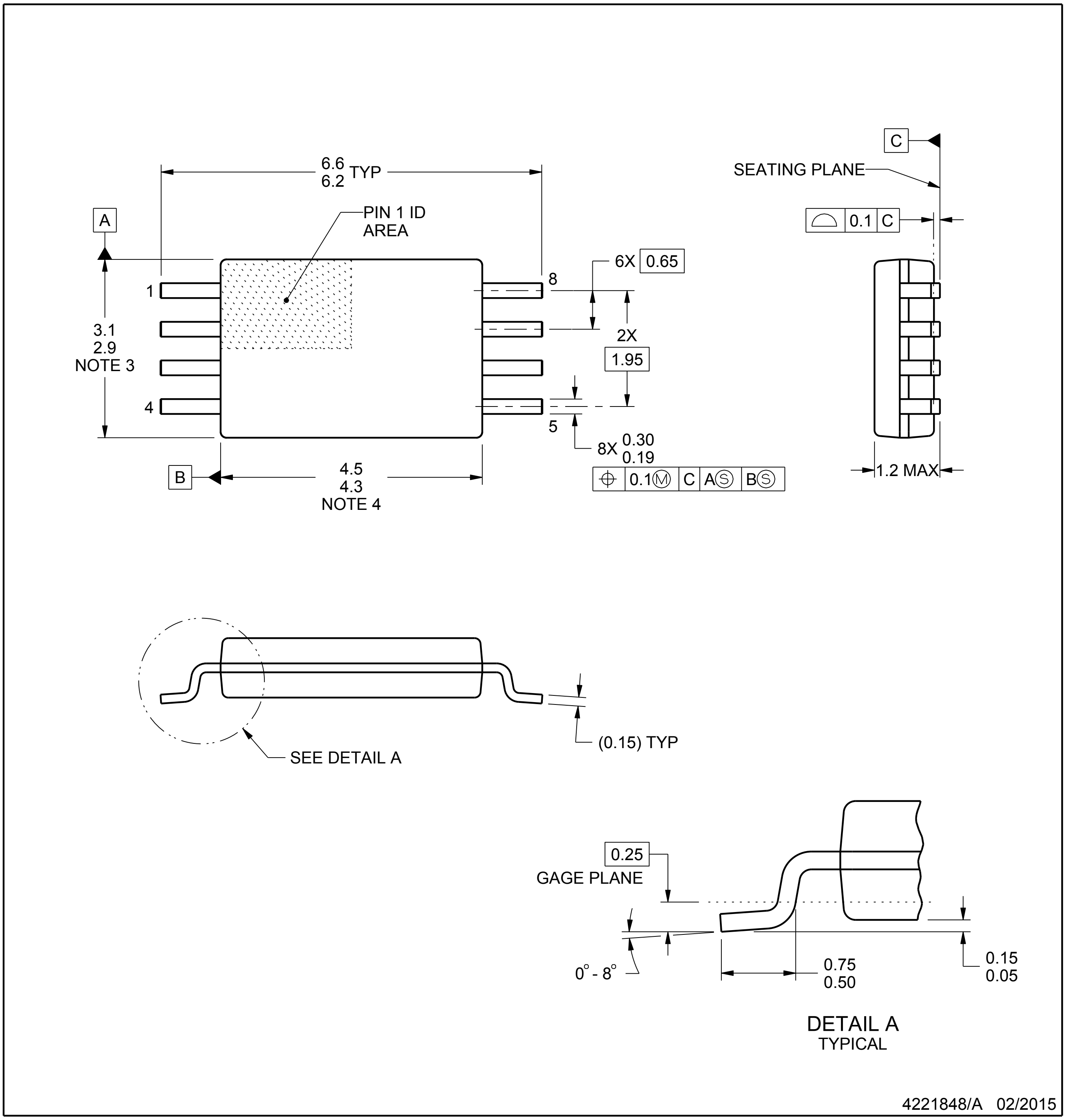
4040049/E 12/2002

NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
- D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

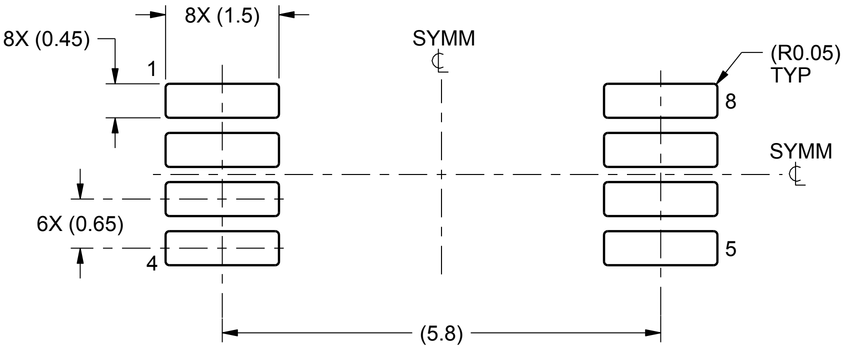
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

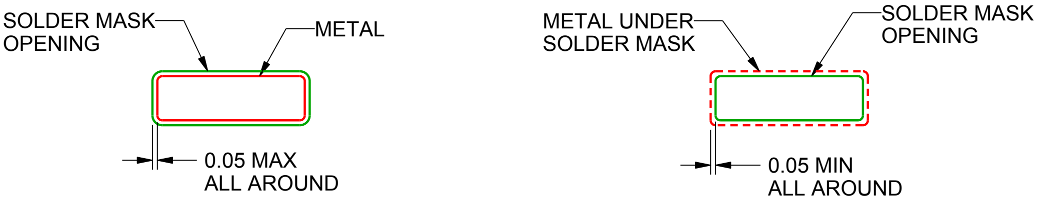


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK
DEFINED

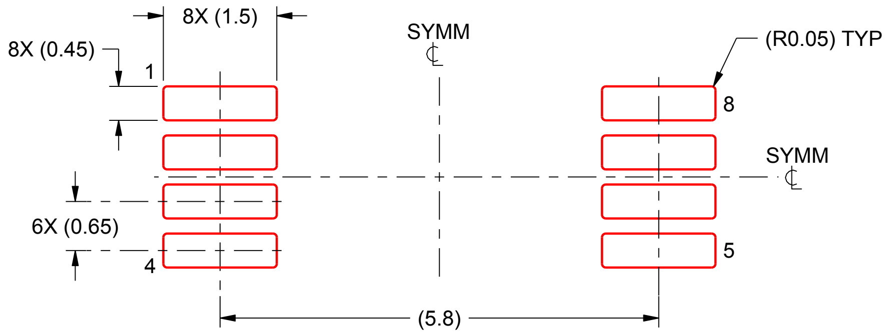
SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

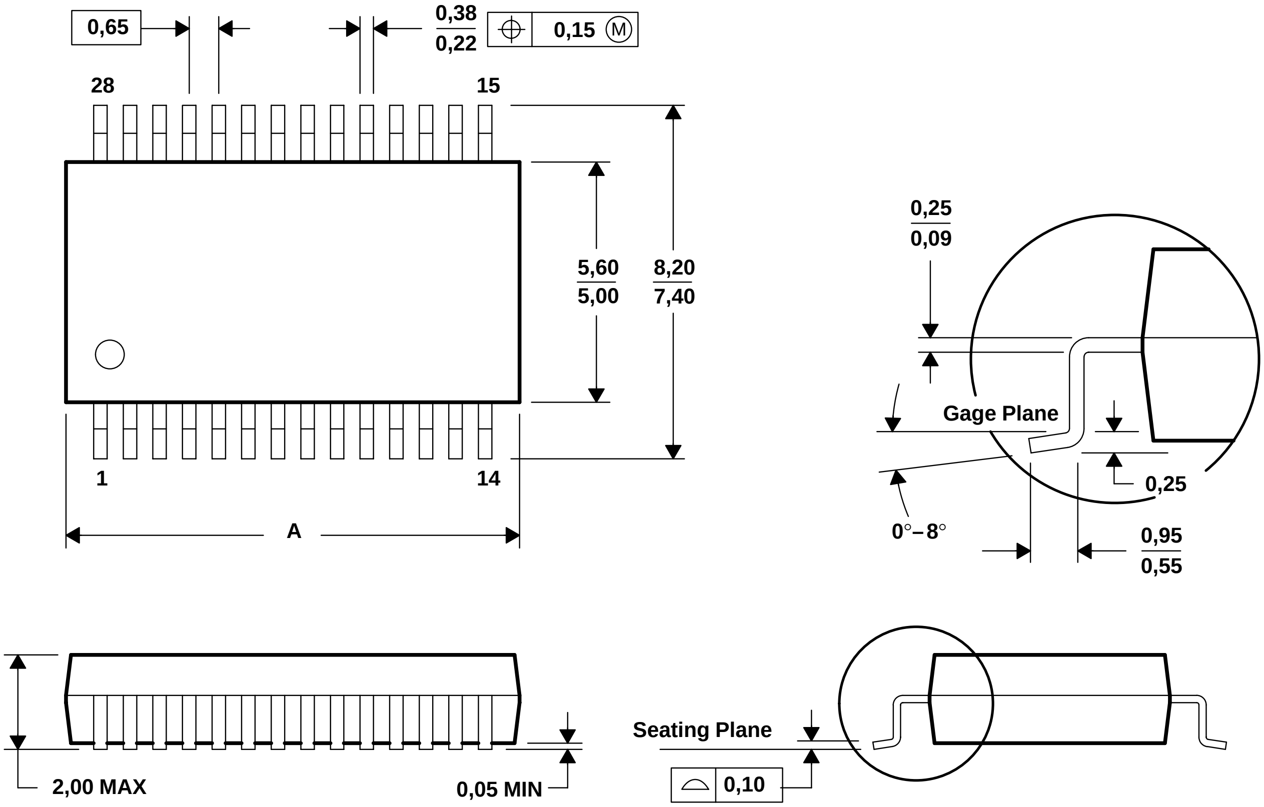
4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G**) PLASTIC SMALL-OUTLINE

28 PINS SHOWN



PINS ** DIM	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

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NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
- D. Falls within JEDEC MO-150

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