Shenzhen Hi-Link Electronic Co.,Ltd

HLK-V21 dual-mic local voice control module

Data sheet

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1. Introduction

1.1. Summary

HLK-V21 local control voice module is the latest set of dual mic human - machine natural voice interaction system developed by Hi-Link for a large number of local control scenes and products. The voice module has rich system peripheral resources, including UART、I2C、SPI、PWM、ADC,etc.

It can be widely and quickly used in smart home, all kinds of intelligent small home appliances, 86 boxes, toys, lamps, industry, medical care, Internet of Things, automobile, security system,lighting and other products that need voice control.

1.2. Features

- Rich peripheral resources, including 4 UART、1 I2C、1 s, SPI、7, PWM、1, ADC、1 SDIO s and up to 23 GPIO，etc
- Support for a 2 - way digital mic or an analog mic
- Maximum power amplifier support 2 65W@4 Ω Or 1 8W@8 Ω
- 59 Pin Stamp hole packaging
- 5 V power supply
- RoHS standard

2. Electrical parameters

2.1. General Technical Specification

Item	Parameters
Working temperature	-20°C to 85°C
Storage temperature	-40°C to 85°C

Working humidity	10% to 95%	No condensation condensation

2.2. Voltage parameters

Power	Min Value	Typical value	Max value	Unit
VCC5V_IN	4.5	5	5.5	V
VCC33_OUT	3.15	3.3	3.45	V

Notes：

1. VCC5V_IN is the input power of module

2. VCC33_OUT is output power,max current is 200mA.

2.3. DC features

Parameters	Description	Min	Typical	Max	Unit
VIL	Input Low Voltage	-	-	0.8	V
VIH	Input High Voltage	2.0	-	-	V
VOL	output Low Voltage	-	-	0.4	V
VOH	output High Voltage	2.4	-	-	V

2.4. ESD features

ITEMS	Description	Value	Unit
V(ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101	±500	V

2.5. Power consumption parameters

working mode	Test condition	consumption	unit
Sleep mode	Sleep to wake up state and unplug mic at the same time	TBD	mW
Active mode	Wake up identification and response status, no horn.	<350	mW

Notes:

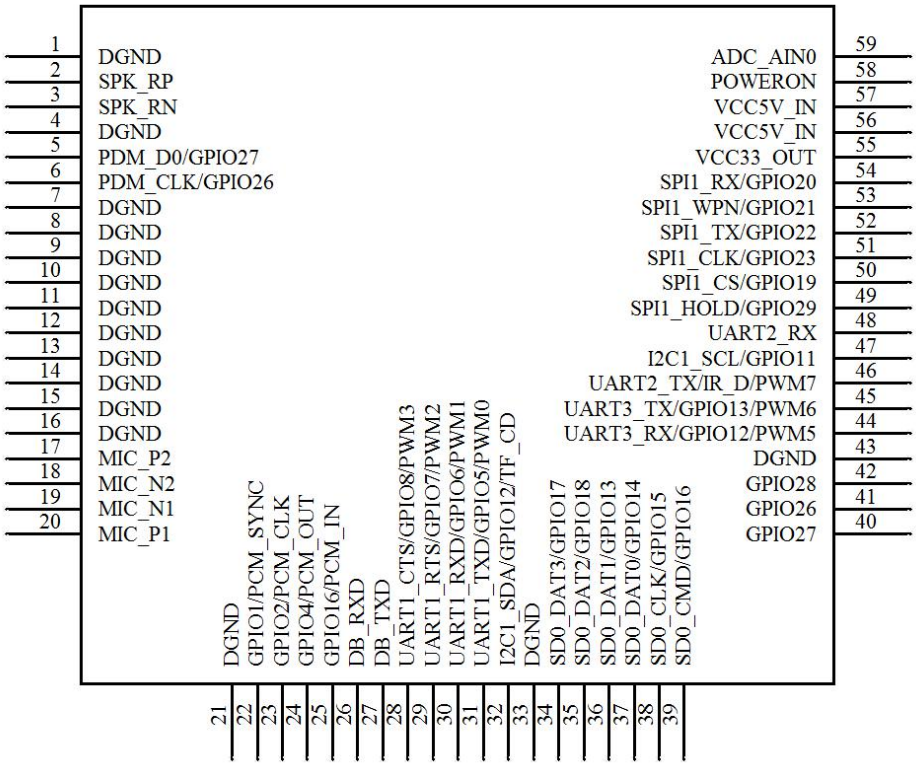
Sleep mode：After normal electricity for a period of time, enter the state to wake up.

Active mode:Power on normally and enter wake-up recognition state.

Power consumption: the test data of different software versions will be different and the data is for reference only.

3. Module pin definition

3.1. Pin definition diagram



HLK-V21 Pin definition diagram

3.2. Default pin chart definition

Pin	Name	Type	Default Status	functional description
1	DGND	Power		DGND
2	SPK_RP	AO		Power amplifier output, maximum 2.65W@4Ωor 1.8W@8
3	SPK_RN	AO		
4	DGND	Power		DGND
5	PDM_D0/GPIO27	I/O	Z	GPIO27Digital MIC Data / Universal GPIO27
6	PDM_CLK/GPIO26	I/O	Z	Digital MIC Clock / Universal GPIO26
7	DGND	Power		DGND
8	DGND	Power		DGND
9	DGND	Power		DGND
10	DGND	Power		DGND
11	DGND	Power		DGND
12	DGND	Power		DGND
13	DGND	Power		DGND
14	DGND	Power		DGND
15	DGND	Power		DGND
16	DGND	Power		DGND
17	MIC_P2	AI		MIC2 Input positive
18	MIC_N2	AI		MIC2 Input negative, single ended input needs to be grounded
19	MIC_N1	AI		The input of mic1 is negative, and the single ended input needs to be grounded
21	DGND	Power		DGND
22	GPIO1/PCM_SYNC	I/O	Z	Universal GPIO1/PCM_SYNC
23	GPIO2/PCM_CLK	I/O	Z	Universal GPIO2/PCM_CLK
24	GPIO4/PCM_OUT	I/O	up	UniversalGPIO4/PCM_OUT
25	GPIO16/PCM_IN	I/O	Z	Universal GPIO16/PCM_IN

26	DB_RXD	I	up	Debug the serial port for receiving the data
27	DB_TXD	O	up	Debug the serial port for receiving the data
28	UART1_CTS/GPIO8/PWM3	I/O	Z	UART1_CTS/ universal GPIO8/PWM3 output
29	UART1_RTS/GPIO7/PWM2	I/O	Z	UART1_RTS/ universal GPIO7/PWM2 output
30	UART1_RXD/GPIO6/PWM1	I/O	up	UART1_RXD/ universal GPIO6/PWM1 output
31	UART1_TXD/GPIO5/PWM0	I/O	up	UART1_TXD/ universal GPIO5/PWM0 output
32	I2C1_SDA/GPIO12/TF_CD	I/O	Z	I2C1_SDA/ universalGPIO12/TFcard detection input
33	DGND	Power		DGND
34	SD0_DAT3/GPIO17	I/O	Z	SDIO_DATA3/Universal GPIO17
35	SD0_DAT2/GPIO18	I/O	Z	SDIO_DATA2/UniversalGPIO18
36	SD0_DAT1/GPIO13	I/O	Z	SDIO_DATA1/UniversalGPIO13
37	SD0_DAT0/GPIO14	I/O	Z	SDIO_DATA0/Universal GPIO14
38	SD0_CLK/GPIO15	I/O	Z	SDIO_CLK/UniversalGPIO15
39	SD0_CMD/GPIO16	I/O	Z	SDIO_CMD/Universal GPIO16
40	GPIO27	I/O	Z	UniversalGPIO27
41	GPIO26	I/O	Z	UniversalGPIO26
42	GPIO28	I/O	Z	Universal GPIO28
43	DGND	Power		DGND
44	UART3_RX/GPIO12/PWM5	I/O	Z	UART3_RX/ universal GPIO12/PWM5 output
45	UART3_TX/GPIO13/PWM6	I/O	Z	UART3_TX/ universal GPIO13/PWM6 output
46	UART2_TX/IR_D/PWM7	I/O	up	UART2_TX/ infrared data reception / PWM7
47	I2C1_SCL/GPIO11	I/O	down	I2C1_SCL/universal GPIO11
48	UART2_RX	I	up	UART2_RX
49	SPI1_HOLD/GPIO29	I/O	Z	SPI1_HOLD/universalGPIO29
50	SPI1_CS/GPIO19	I/O	up	SPI1_CS/universalGPIO19
51	SPI1_CLK/GPIO23	I/O	Z	SPI1_CLK/universal GPIO23
52	SPI1_TX/GPIO22	I/O	Z	SPI1_TX/universalGPIO22
53	SPI1_WPN/GPIO21	I/O	down	SPI1_WPN/universalGPIO21
54	SPI1_RX/GPIO20	I/O	up	SPI1_RX/universal GPIO20

55	VCC33_OUT	Power		3.3V POWER output，Max 0.2A
56	VCC5V_IN	Power		5V input
57	VCC5V_IN	Power		
58	POWERON	I	up	Power enable 1：High level power: 0：Low level down. It can be suspended when not in use
59	ADC_AIN0	AI		ADC voltage detection input

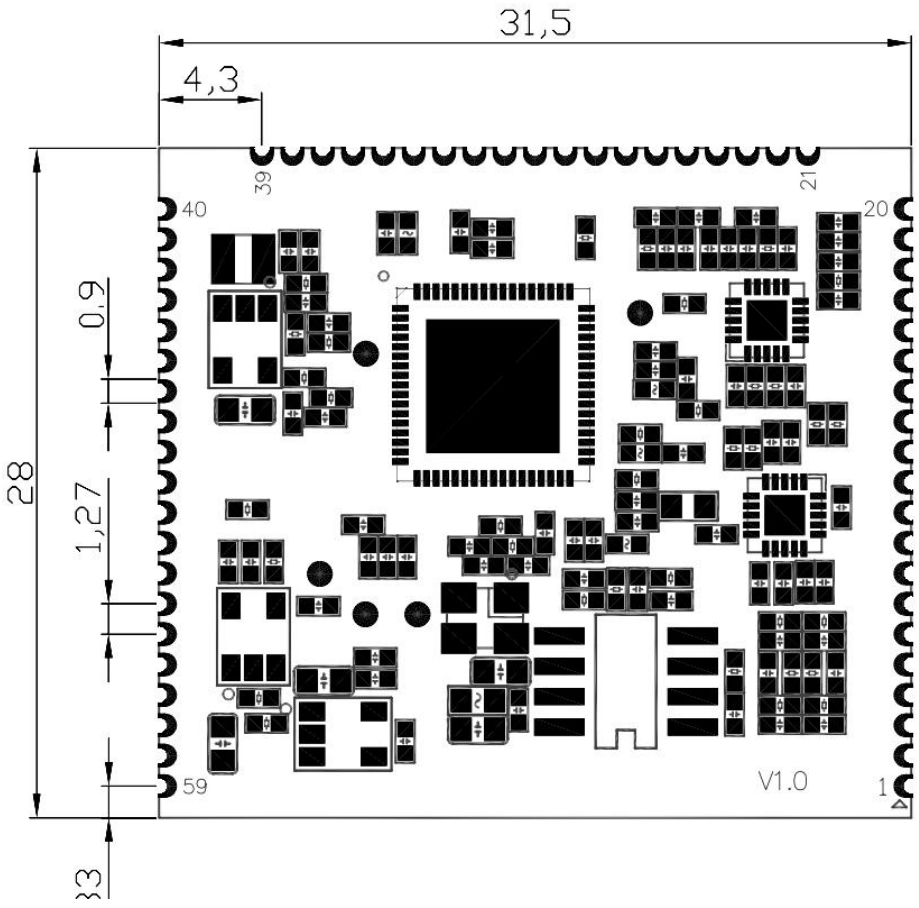
Notes：

1，Type: I=input;O=output;I/O=input/output(bidirectional); AO=Analog output;AI=Analog input。。

2，Default status: up=pull up;down=pull down;Z= high-Z。

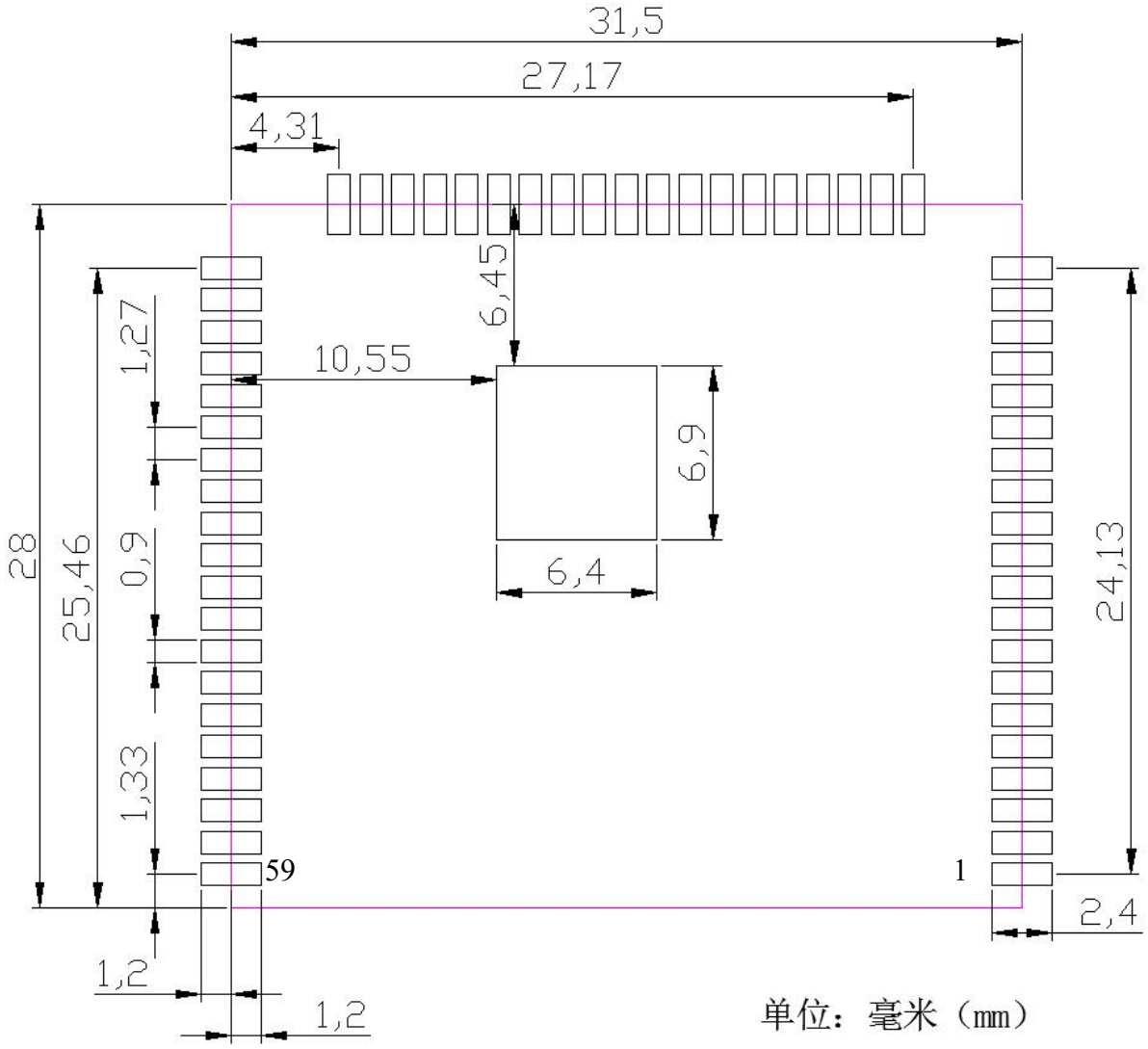
4. Module size

4.1. Dimension



Unit: mm

4.2. Package dimension diagram



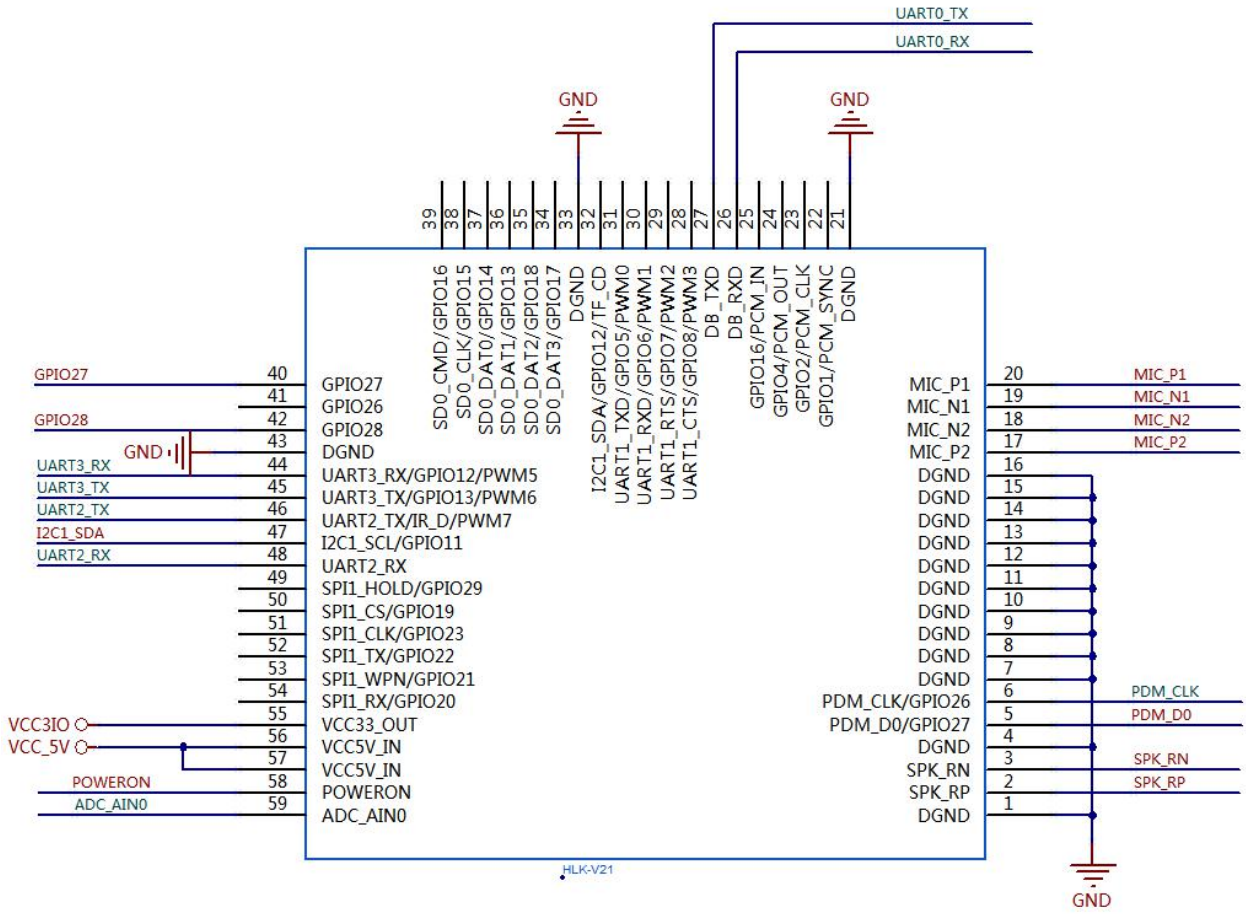
Layout Recommended packaging dimensions（Top view）

Notes：

1. The intermediate hot pad is grounded.

2. Total height of module: 2.8mm.

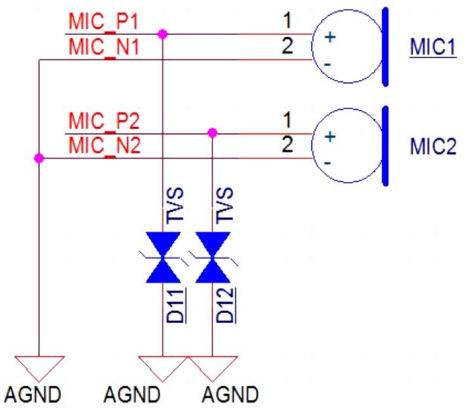
5. Reference Circuit design



Module Schematics

5.1. Microphone reference circuit

5.1.1. Analog microphone reference circuit



Analog microphone reference circuit

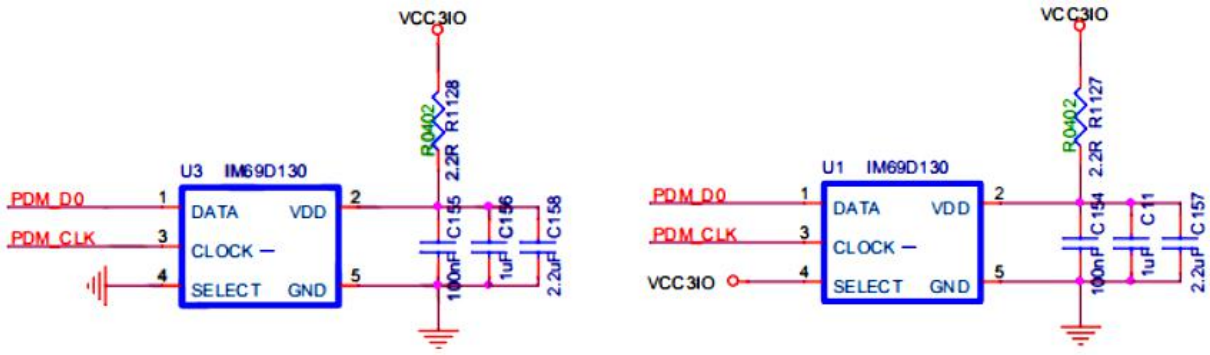
Notes:

1. “MIC_ N1 "and" mic "_ The "N2" network must be grounded when using a single ended analog

microphone.

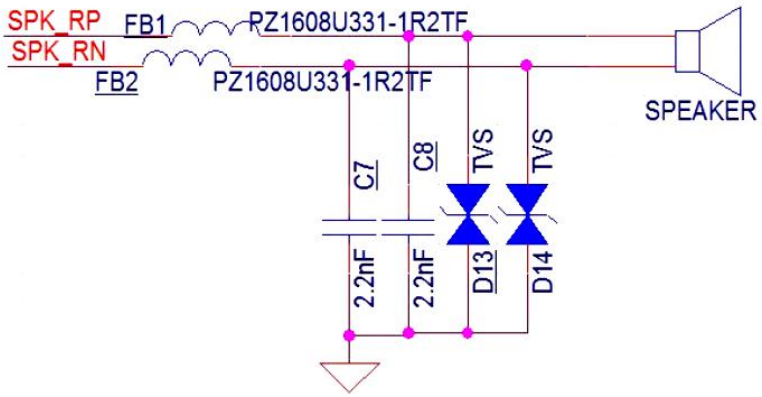
2. ESD protection needs to be increased or decreased according to customer product requirements.

5.1.2. Digital microphone reference circuit



Digital microphone reference circuit

5.2. Speaker reference circuit



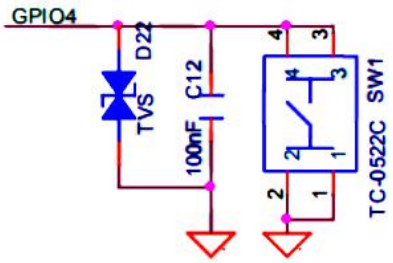
Notes:

1. FB1, FB2 and C7, C8 are mainly used for EMI testing, which can be deleted according to the test needs.

2. ESD protection needs to be retained according to customer product requirements.

5.3. Debugging circuit

5.3.1. Download Mode



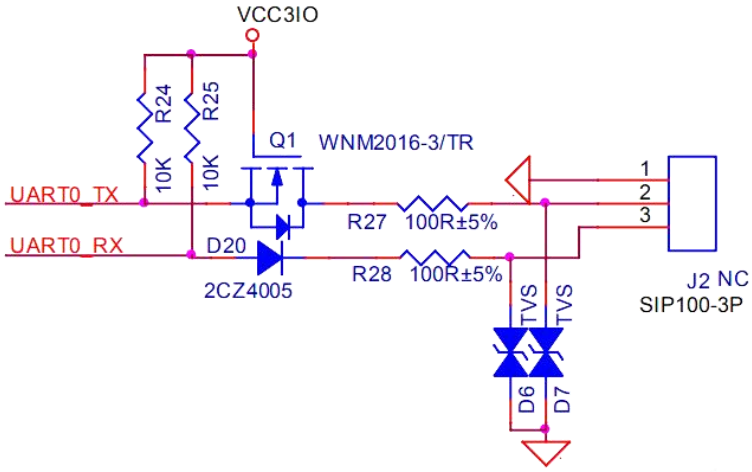
Download mode

By pressing the key to pull down gpio4, the voice core module can enter the download mode, and the program can be burned through serial port 0.

Notes:

1. Gpio4 has done pull-up processing on the voice core module.
2. ESD protection should be added.

5.3.2. Debug serial reference circuit



Debug the serial reference circuit

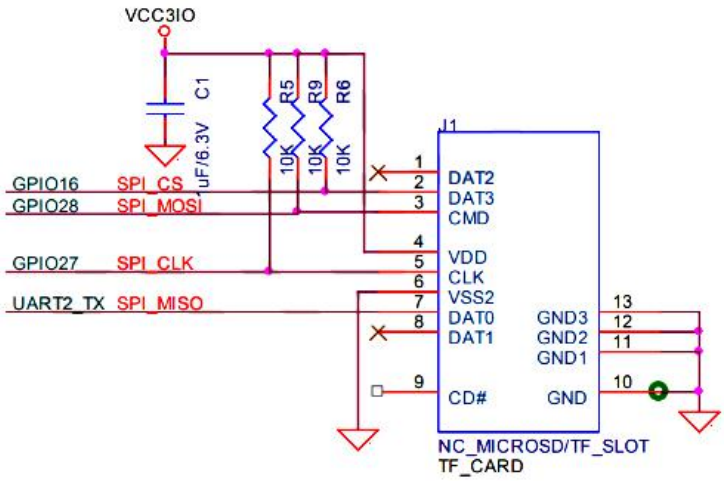
Serial port 0 is the debugging serial port, through which you can download programs, view logs and other debugging operations.

Notes:

1. Q1 and D20 constitute anti leakage circuit. This circuit can prevent the voice module from being abnormal due to the leakage of the third-party debugging serial module before power on, so it is recommended to keep it without great cost pressure.

2.R27, R28 and ESD protection need to be retained according to customer product requirements.

5.4. TF Card reference circuit

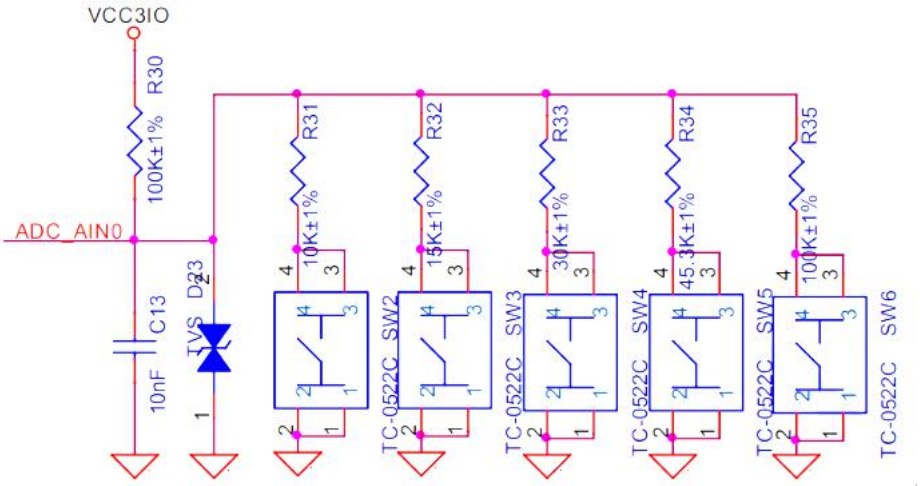


TF Card reference circuit

Notes:

If the function of TF card is not needed by the customer, it is recommended to keep the relevant circuit on the PCB to facilitate the debug use of subsequent products and the components can be pasted empty.

5.5. Key reference circuit



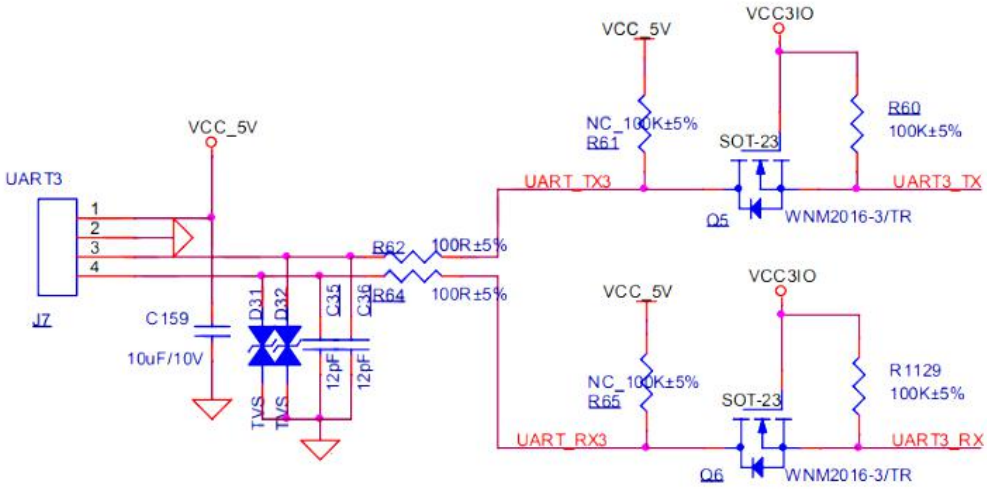
Key reference circuit

Notes:

1. Please design in strict accordance with the resistance value of the reference design.
2. The resistance needs to use precision resistance, that is, the precision is 1%.

3. The reference design is 5 buttons, customers can make corresponding increase or decrease according to the actual needs of the product.

5.6. Communication serial port reference circuit



Communication serial port reference circuit

The voice core module provides four serial ports, of which serial port 0 is used as the debugging serial port, and the priority of the other three serial ports is recommended as serial port 3, serial port 1, and serial port 2.

Notes:

1. Q5, Q6 constitute the serial port transceiver level conversion, the customer can decide whether to retain according to the product requirements.

2.R62, R64 and C35, C36 are mainly used for EMI test, which can be deleted according to the test needs.

3. ESD protection needs to be increased or decreased according to customer product requirements.

6. Reference reflow temperature curve

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times