

# Designer's™ Data Sheet

## Insulated Gate Bipolar Transistor

### N-Channel Enhancement-Mode Silicon Gate

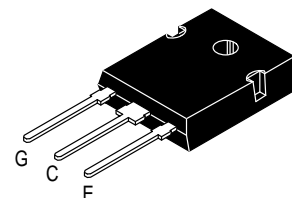
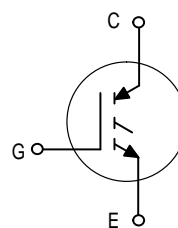
**MGW12N120**

Motorola Preferred Device

This Insulated Gate Bipolar Transistor (IGBT) uses an advanced termination scheme to provide an enhanced and reliable high voltage-blocking capability. Short circuit rated IGBT's are specifically suited for applications requiring a guaranteed short circuit withstand time such as Motor Control Drives. Fast switching characteristics result in efficient operation at high frequencies.

**IGBT IN TO-247**  
**12 A @ 90°C**  
**20 A @ 25°C**  
**1200 VOLTS**  
**SHORT CIRCUIT RATED**

- Industry Standard High Power TO-247 Package with Isolated Mounting Hole
- High Speed  $E_{off}$ : 160  $\mu$ J/A typical at 125°C
- High Short Circuit Capability – 10  $\mu$ s minimum
- Robust High Voltage Termination



CASE 340F-03, Style 4  
TO-247AE

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CES}$	1200	Vdc
Collector-Gate Voltage ( $R_{GE} = 1.0 \text{ M}\Omega$ )	$V_{CGR}$	1200	Vdc
Gate-Emitter Voltage — Continuous	$V_{GE}$	$\pm 20$	Vdc
Collector Current — Continuous @ $T_C = 25^\circ\text{C}$ — Continuous @ $T_C = 90^\circ\text{C}$ — Repetitive Pulsed Current (1)	$I_{C25}$ $I_{C90}$ $I_{CM}$	20 12 40	Adc Apk
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	123 0.98	Watts W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-55 to 150	°C
Short Circuit Withstand Time ( $V_{CC} = 720 \text{ Vdc}$ , $V_{GE} = 15 \text{ Vdc}$ , $T_J = 125^\circ\text{C}$ , $R_G = 20 \Omega$ )	$t_{sc}$	10	$\mu$ s
Thermal Resistance — Junction to Case – IGBT — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 45	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	$T_L$	260	°C
Mounting Torque, 6-32 or M3 screw		10 lbf•in (1.13 N•m)	

(1) Pulse width is limited by maximum junction temperature. Repetitive rating.

**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

**Preferred** devices are Motorola recommended choices for future use and best overall value.

# MGW12N120

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-to-Emitter Breakdown Voltage (V <sub>GE</sub> = 0 Vdc, I <sub>C</sub> = 25 μAdc) Temperature Coefficient (Positive)	BV <sub>CES</sub>	1200 —	— 870	— —	Vdc mV/°C
Emitter-to-Collector Breakdown Voltage (V <sub>GE</sub> = 0 Vdc, I <sub>EC</sub> = 100 mAdc)	BV <sub>ECS</sub>	25	—	—	Vdc
Zero Gate Voltage Collector Current (V <sub>CE</sub> = 1200 Vdc, V <sub>GE</sub> = 0 Vdc) (V <sub>CE</sub> = 1200 Vdc, V <sub>GE</sub> = 0 Vdc, T <sub>J</sub> = 125°C)	I <sub>CES</sub>	— —	— —	100 2500	μAdc
Gate-Body Leakage Current (V <sub>GE</sub> = ± 20 Vdc, V <sub>CE</sub> = 0 Vdc)	I <sub>GES</sub>	—	—	250	nAdc

## ON CHARACTERISTICS (1)

Collector-to-Emitter On-State Voltage (V <sub>GE</sub> = 15 Vdc, I <sub>C</sub> = 5.0 Adc) (V <sub>GE</sub> = 15 Vdc, I <sub>C</sub> = 5.0 Adc, T <sub>J</sub> = 125°C) (V <sub>GE</sub> = 15 Vdc, I <sub>C</sub> = 10 Adc)	V <sub>CE(on)</sub>	— — —	2.51 2.36 3.21	3.37 — 4.42	Vdc
Gate Threshold Voltage (V <sub>CE</sub> = V <sub>GE</sub> , I <sub>C</sub> = 1.0 mAdc) Threshold Temperature Coefficient (Negative)	V <sub>GE(th)</sub>	4.0 —	6.0 10	8.0 —	Vdc mV/°C
Forward Transconductance (V <sub>CE</sub> = 10 Vdc, I <sub>C</sub> = 10 Adc)	g <sub>fe</sub>	—	12	—	Mhos

## DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>CE</sub> = 25 Vdc, V <sub>GE</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>ies</sub>	—	930	—	pF
Output Capacitance		C <sub>oes</sub>	—	126	—	
Transfer Capacitance		C <sub>res</sub>	—	16	—	

## SWITCHING CHARACTERISTICS (1)

Turn-On Delay Time	(V <sub>CC</sub> = 720 Vdc, I <sub>C</sub> = 10 Adc, V <sub>GE</sub> = 15 Vdc, L = 300 μH R <sub>G</sub> = 20 Ω, T <sub>J</sub> = 25°C) Energy losses include "tail"	t <sub>d(on)</sub>	—	74	—	ns
Rise Time		t <sub>r</sub>	—	83	—	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	76	—	
Fall Time		t <sub>f</sub>	—	231	—	
Turn-Off Switching Loss		E <sub>off</sub>	—	0.55	1.33	
Turn-On Delay Time	(V <sub>CC</sub> = 720 Vdc, I <sub>C</sub> = 10 Adc, V <sub>GE</sub> = 15 Vdc, L = 300 μH R <sub>G</sub> = 20 Ω, T <sub>J</sub> = 125°C) Energy losses include "tail"	t <sub>d(on)</sub>	—	66	—	ns
Rise Time		t <sub>r</sub>	—	87	—	
Turn-Off Delay Time		t <sub>d(off)</sub>	—	120	—	
Fall Time		t <sub>f</sub>	—	575	—	
Turn-Off Switching Loss		E <sub>off</sub>	—	1.49	—	
Gate Charge	(V <sub>CC</sub> = 720 Vdc, I <sub>C</sub> = 10 Adc, V <sub>GE</sub> = 15 Vdc)	Q <sub>T</sub>	—	31	—	nC
		Q <sub>1</sub>	—	13	—	
		Q <sub>2</sub>	—	14	—	

## INTERNAL PACKAGE INDUCTANCE

Internal Emitter Inductance (Measured from the emitter lead 0.25" from package to emitter bond pad)	L <sub>E</sub>	—	13	—	nH
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(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

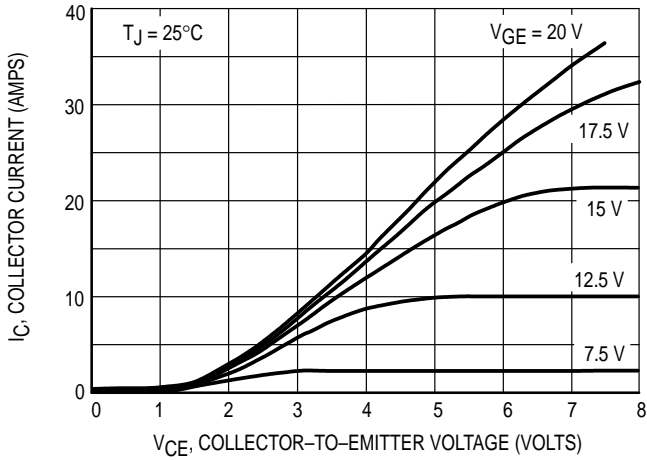


Figure 1. Output Characteristics,  $T_J = 25^\circ\text{C}$

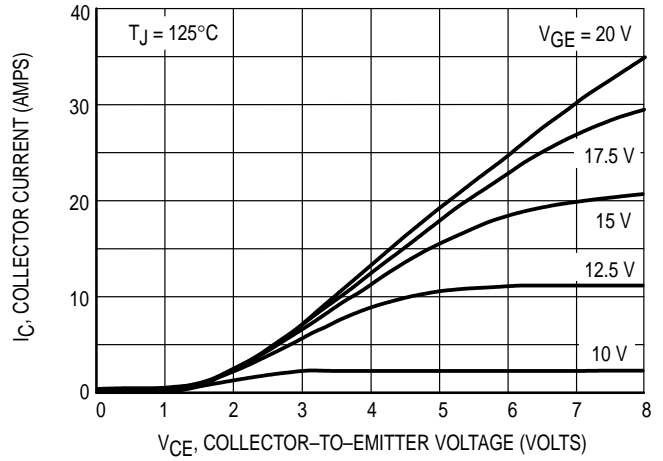


Figure 2. Output Characteristics,  $T_J = 125^\circ\text{C}$

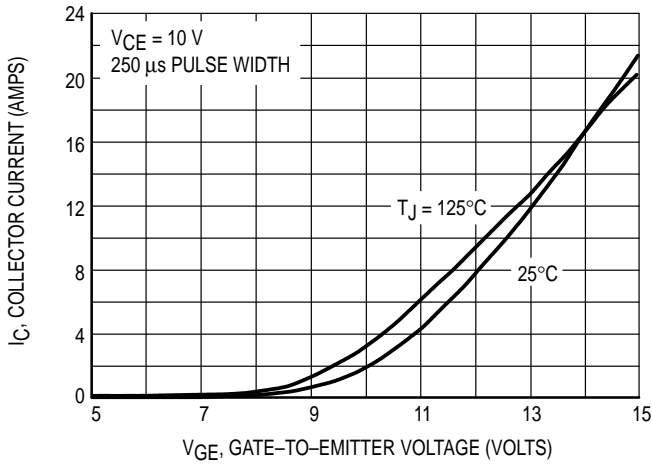


Figure 3. Transfer Characteristics

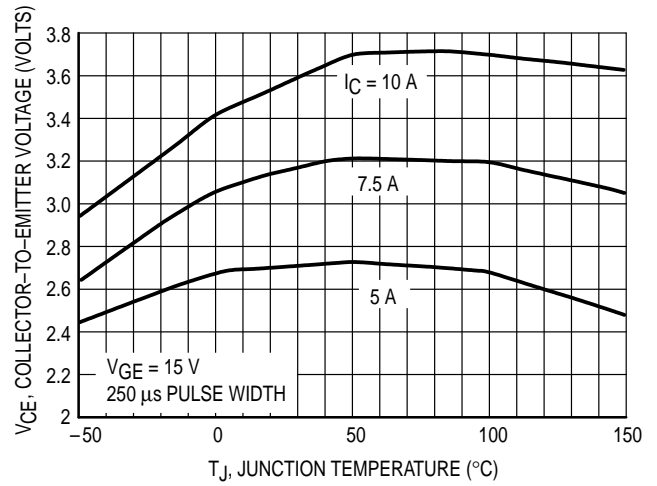


Figure 4. Collector-to-Emitter Saturation Voltage versus Junction Temperature

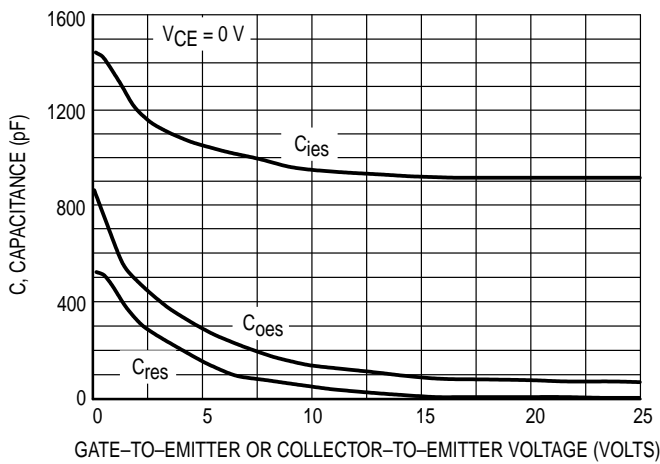


Figure 5. Capacitance Variation

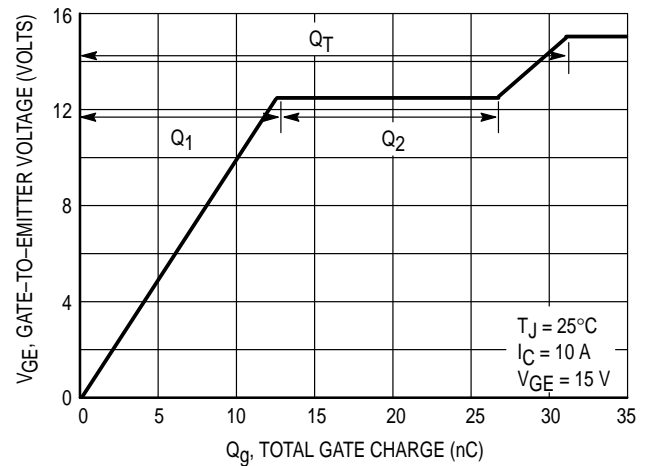
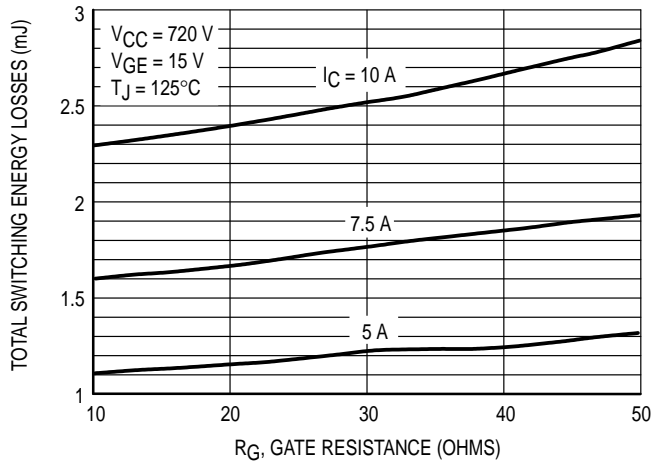
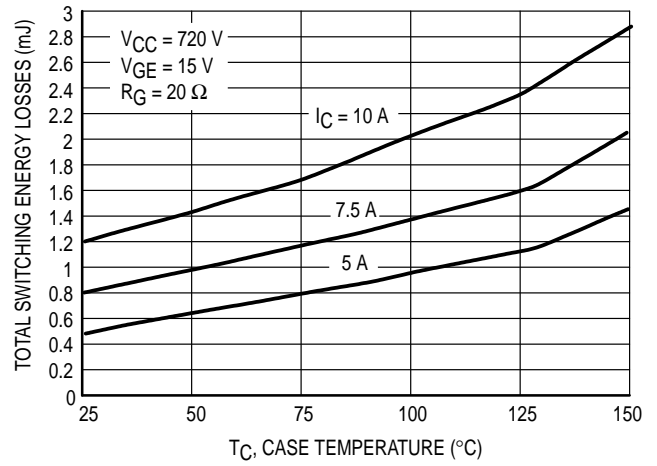


Figure 6. Gate-to-Emitter Voltage versus Total Charge

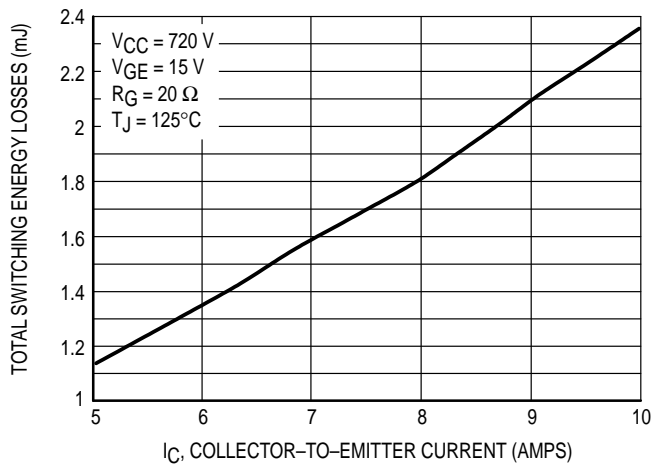
# MGW12N120



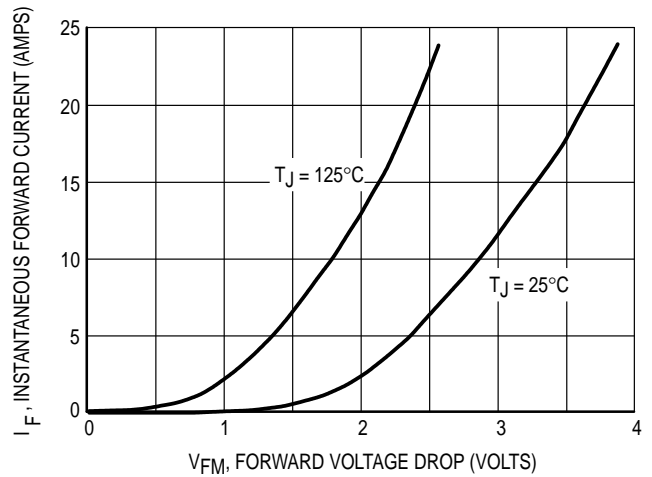
**Figure 7. Total Switching Losses versus Gate Resistance**



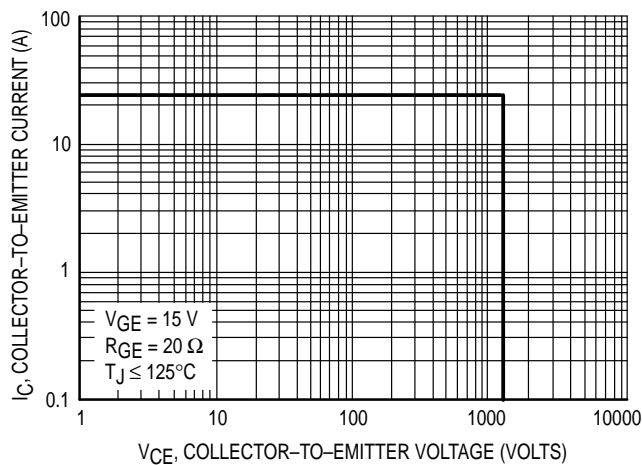
**Figure 8. Total Switching Losses versus Case Temperature**



**Figure 9. Total Switching Losses versus Collector-to-Emitter Current**



**Figure 10. Maximum Forward Drop versus Instantaneous Forward Current**



**Figure 11. Reverse Biased Safe Operating Area**

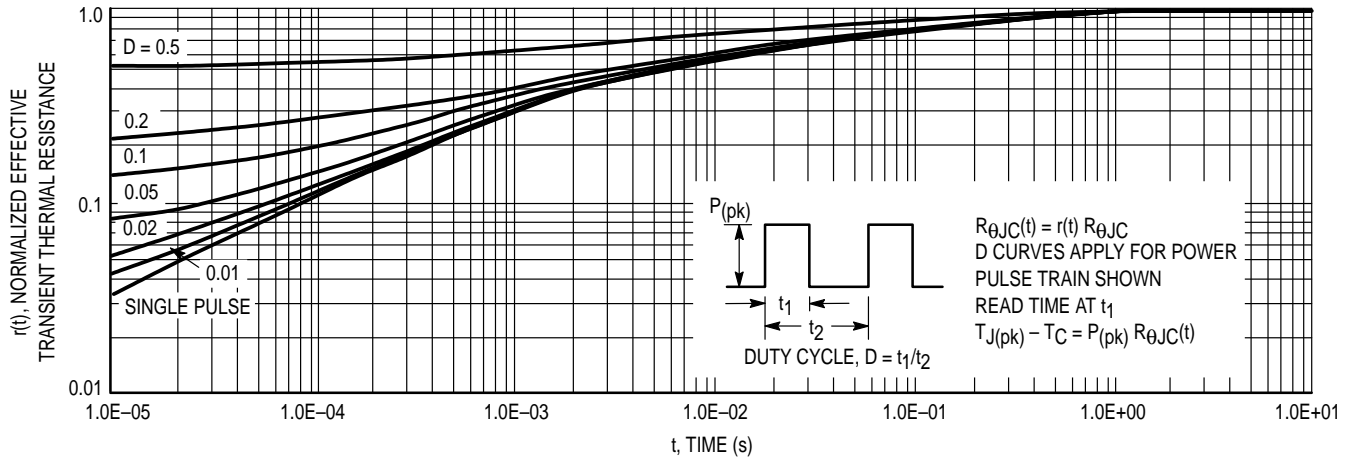
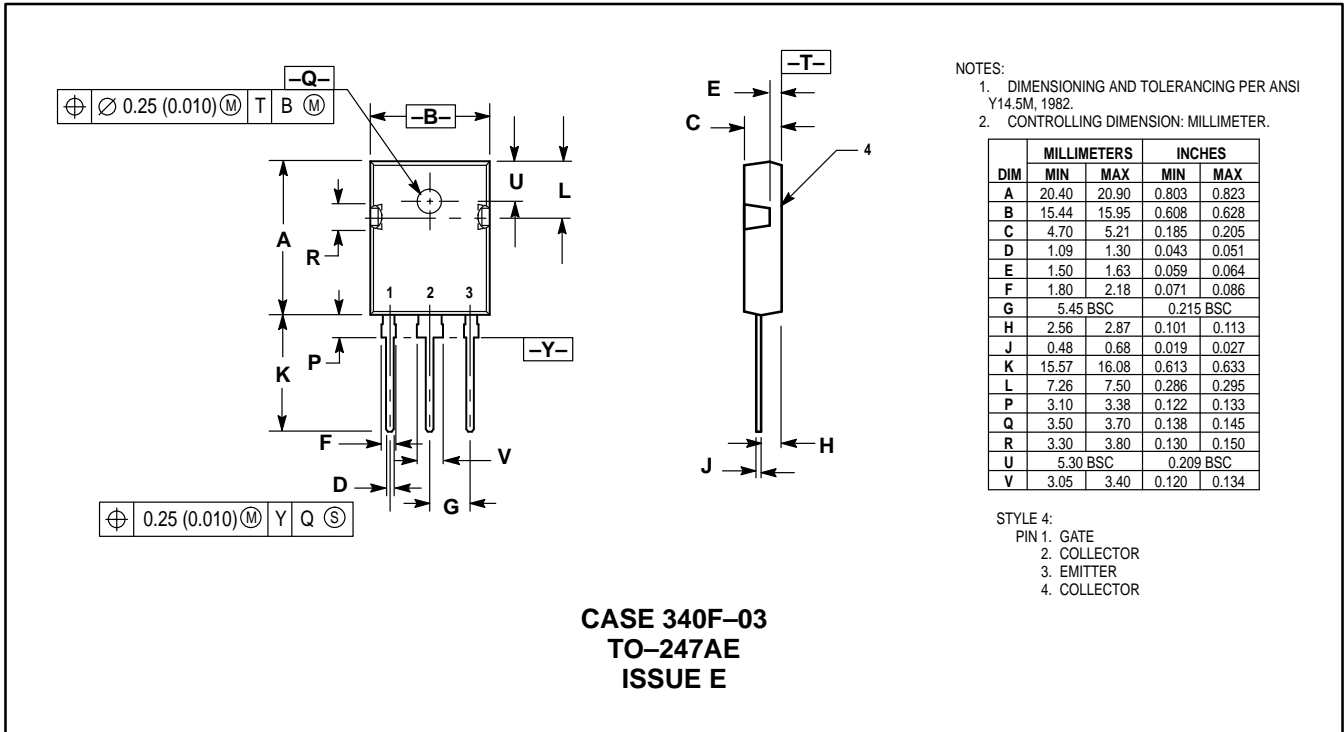


Figure 12. Thermal Response

PACKAGE DIMENSIONS



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**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

**MFAX:** RMFA00@email.sps.mot.com – TOUCHTONE 602-244-6609  
**INTERNET:** http://Design-NET.com

**ASIA/PACIFIC:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298



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