EG27324 Datasheet

Dual driver chip with SD function

REV 1.0

Version Change record

Version №	Date	Description
V1.0	January 10, 2018	EG27324 first draft Datasheet

Contents

EG27324 Datasheet V1.0

1. Features

- Adapt to 5V, 3.3V input voltage
- VCC voltage range 2.8V-20V
- Output current capability IO+/- 2A/2.5A
- Short input and output delay
- SD input channel is active at high level, and HO and LO outputs are closed.
- Few peripheral components
- Quiescent current is less than 1uA, very suitable for battery occasions
- Package form: SOP-8

2. Description

The EG27324 is a cost-effective, dual independent driver dedicated chip with SD function.Internal integration of logic signal input processing circuit,level shift circuit,output drive circuit for motor controller, power supply, transformer drive circuit.

The EG27324 has a wide supply voltage range of 2.8 V~20V and a quiescent power consumption of less than 1uA.The chip input channel INA and INB each built - in a 200k pull-down resistor; SD built-in a 200k pull-down resistor,when the SD input is floating, does not affect the output of OUTA and OUTB; output current capability IO+/ - 2/2.5 A; using SOP8 package.

3. Application areas

- Power bank
- Variable frequency pump controller
- Power supply
- Wireless charging driver
- Motor driver
- Drive transformer

4. Pin

4.1 Pin definition

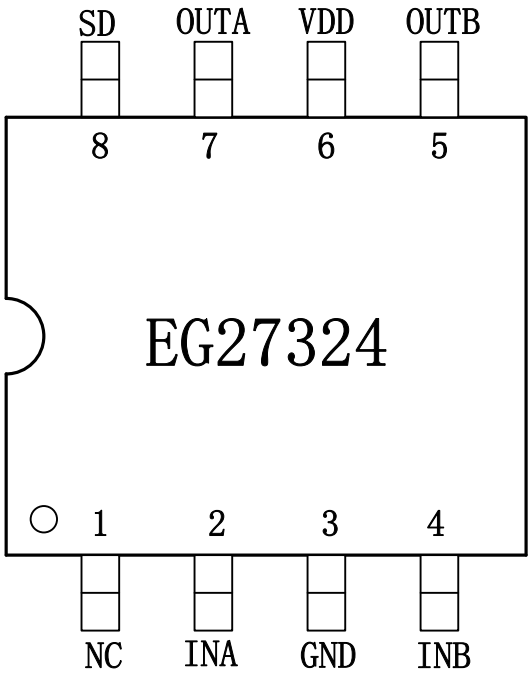

Figure 4-1. EG27324 pin definition

4.2 Pin description

Pin serial №	Pin name	I/O	Description
1	NC	NC	NC
2	INA	I	Logic input control signal, control output OUTA. "0" corresponds to the OUTA low level. "1" corresponds to the OUTA high level.
3	GND	GND	The ground end of the chip.
4	INB	I	Logic input control signal, control output OUTB. "0" corresponds to the OUTB low level. "1" corresponds to the OUTB high level.
5	OUTB	O	B output pin.
6	VDD	power	Chip power supply.
7	OUTA	O	A output pin.
8	SD	I	Logic input control signal active high, forcing the OUTA,OUTB output low. "0" allows OUTA, OUTB with INA, INB input control. "1" forces the OUTA, OUTB outputs low.

5. Block diagram

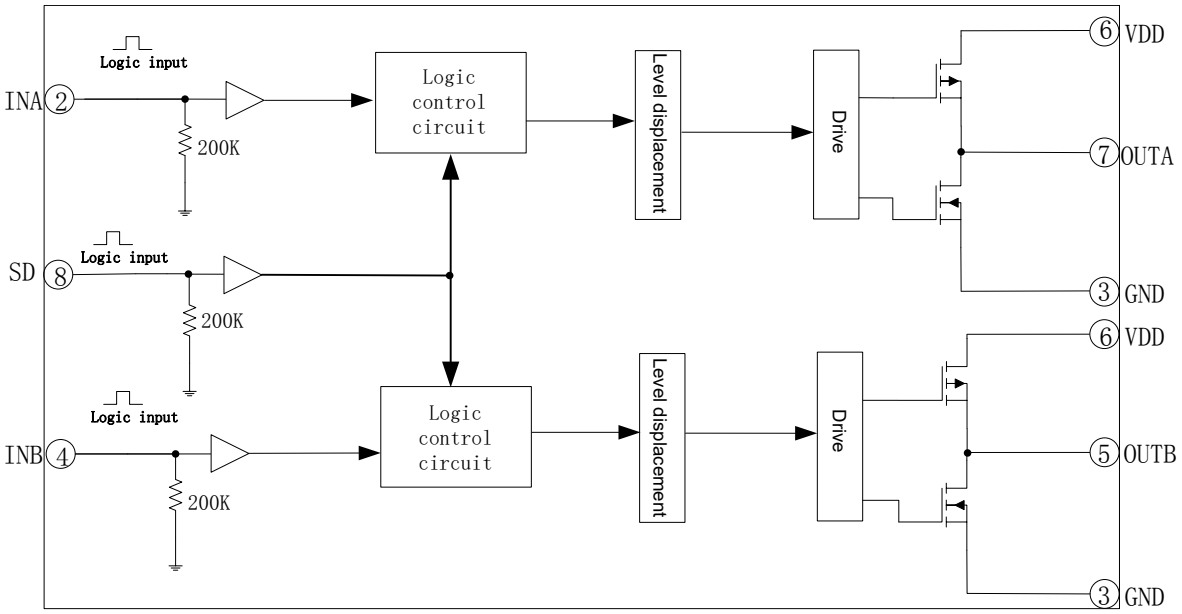

Figure 5-1. EG27324 internal circuit diagram

6. Typical application circuit

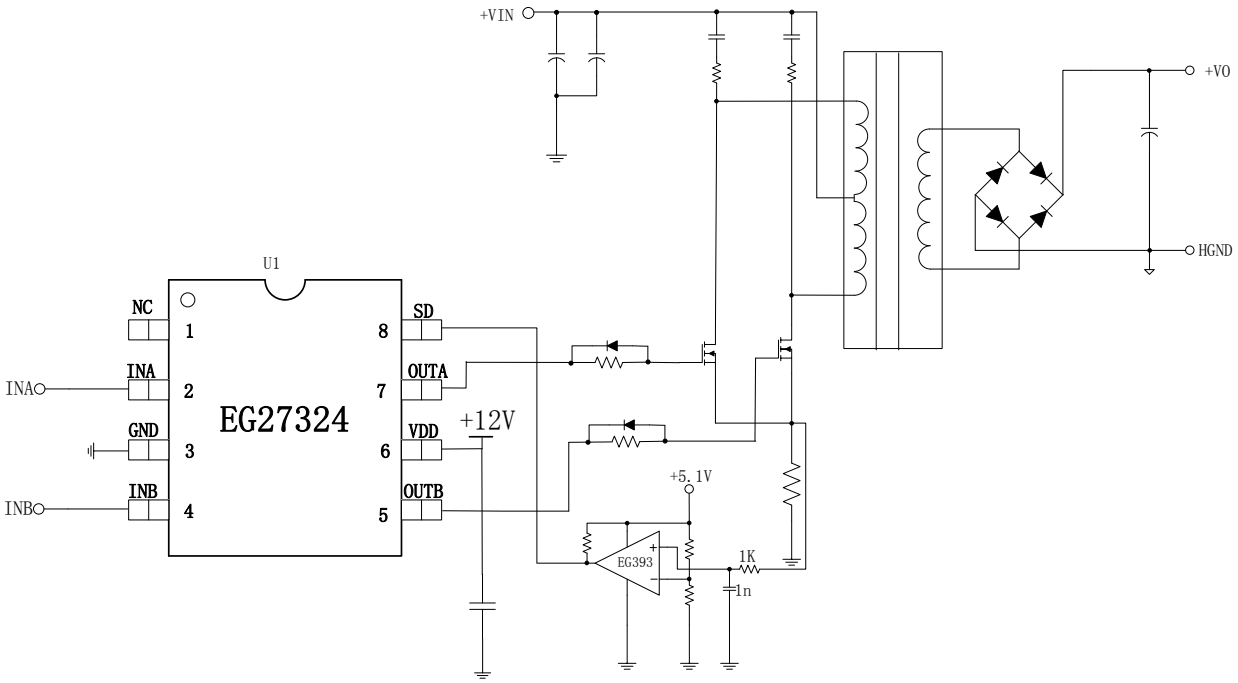

Figure 6-1. EG27324 typical application circuit diagram

7. Electrical characteristics

7.1 Limit parameters

Without further explanation, at TA=25℃ conditions

Symbols	Parameter name	Test conditions	Min.	Max.	Units
Output	OUTA、OUTB	-	-0.3	VDD+0.3	V
Power supply	VDD	-	-0.3	20	V
Logic signal input level	INA、INB、SD	-	-0.3	20	V
TA	Ambient temperature	-	-45	125	℃
Tstr	Storage temperature	-	-55	150	℃
TL	Soldering temperature	T=10S	-	300	℃

Note: exceeding the listed limit parameters may cause permanent damage to the chip, operating in extreme conditions for a long time will affect the reliability of the chip.

7.2 Typical parameters

Without further explanation, at TA=25℃, VCC=12V, load capacitance CL=1NF conditions

Parameter name	Symbols	Test conditions	Min.	Typical	Max.	Units
Power supply	Vcc	-	2.8	12	20	V
Quiescent current	Icc	Input floating, VCC=12V	-	-	1	uA
Input logic signal high potential	Vin(H)	All input control signals	2.5	-	-	V
Input logic signal low potential	Vin(L)	All input control signals	-0.3	0	1.0	V
Current at the high level of the input logic signal	Iin(H)	Vin=5V	-	-	30	uA
Input logic signal low current	Iin(L)	Vin=0V	-10	-	-	uA
Low-side output LO switching time characteristics						
On delay	Ton	See Figure 7-1	-	80	150	ns
Off delay	Toff	See Figure 7-1	-	60	100	ns
Rise Time	Tr	See Figure 7-1	-	40	100	ns
Descent time	Tf	See Figure 7-1	-	20	50	ns
IO output maximum drive capability						
IO output pull current	IO+	Vo=0V,VIN=VIH PW≤10uS	1.5	2	-	A
IO output sink current	IO-	Vo=12V,VIN=VIL PW≤10uS	2	2.5	-	A

7.3 Switching time waveform diagram

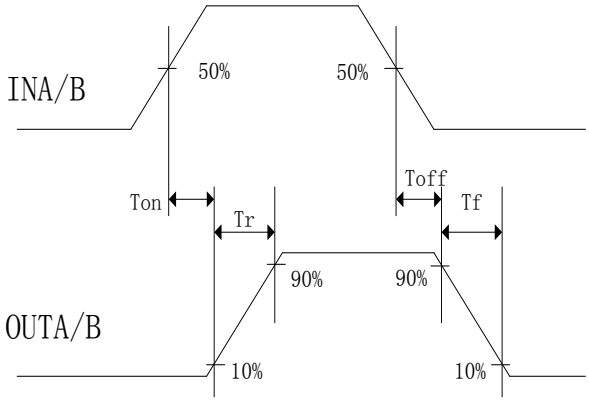

Figure 7-1. Output LO switching time waveform diagram

7.4 Input-output logic

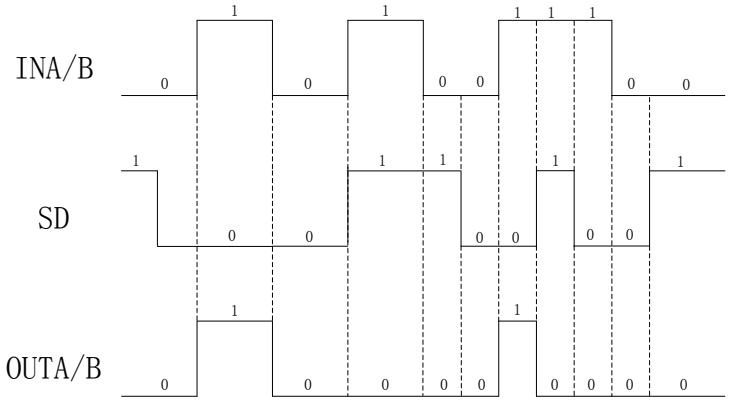

Figure 7-2. Input signal and output signal logic function diagram

Logic truth table for input and output signals：

Input			Output	
Input and output logic				
INA	INB	SD	OUTA	OUTB
0	0	0	0	0
0	1	0	0	1
1	0	0	1	0
1	1	0	1	1
1 or 0	1 or 0	1	0	0

From the truth table, when the input logic signal SD is "1“, regardless of INA, INB is ”1“ or ”0“, the chip output OUTA, OUTB at the same time ”0".

8. Package size

8.1 SO8 Package size